2013 S-Series Intel Shark Bay

UMA/DIS Muxless Schematic
14.0"Rampage 15.6"Renegade 17.0"Ricochet

Haswell-M Dual/Quad Core SV
rPGA947 37W
Lynx Point-M PCH

REV:MV

2013-08-01

DY:No stuff

DIS_PX:Only DIS install

<Core Design>

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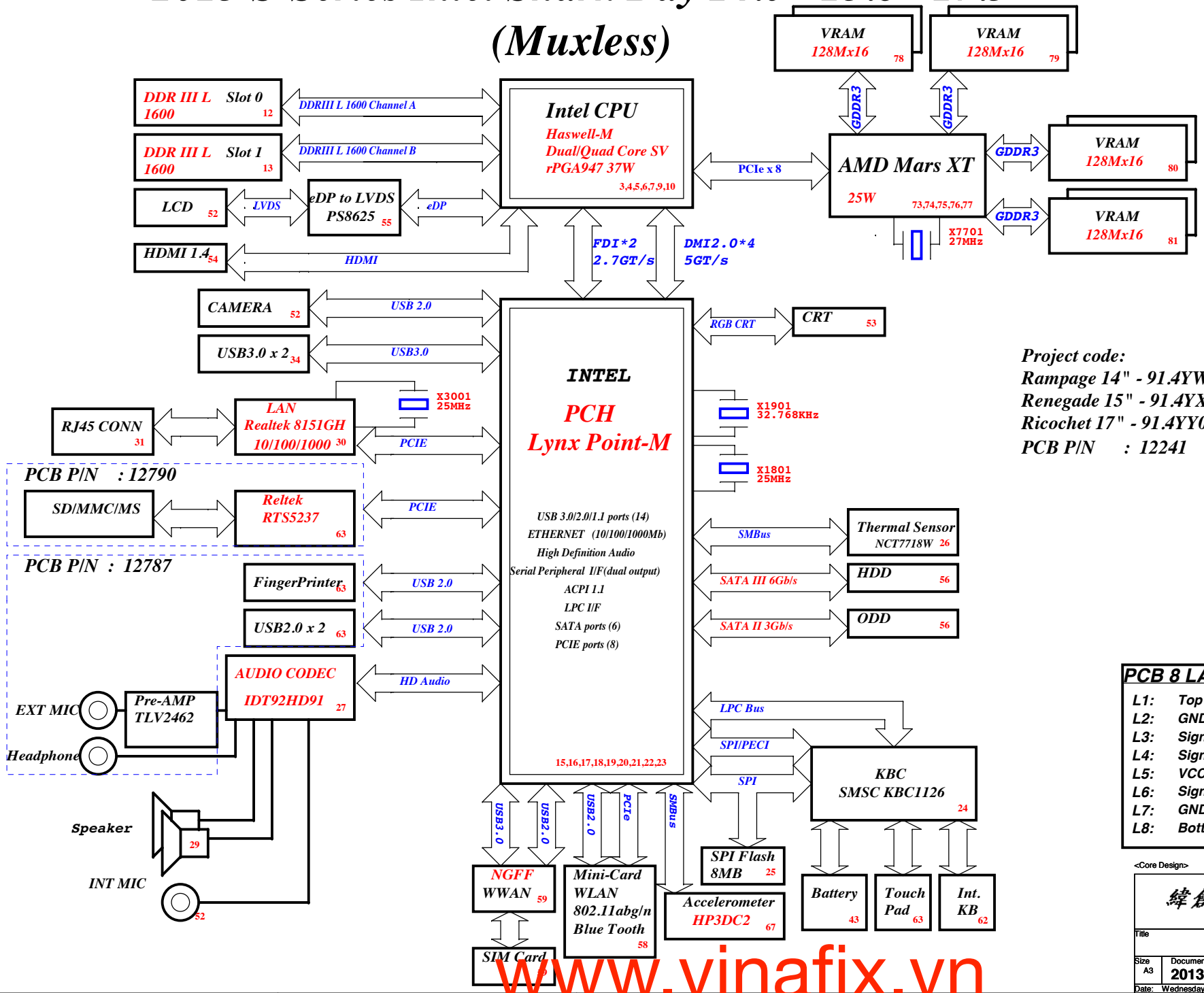
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size	Document Number	Rev
A4	2013 S-Series Shark Bay 14 15 17	1

Date: Thursday, August 01, 2013 Sheet 1 of 103

2013 S-Series Intel Shark Bay 14.0" 15.6" 17.3"
(Muxless)



Project code:
Rampage 14" - 91.4YW01.001
Renegade 15" - 91.4YX01.001
Ricochet 17" - 91.4YY01.001
PCB P/N : 12241

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

CPU DC/DC TPS51631RSMR 46,47

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51367RVER 48

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8223MZQW 45

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 49

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3

SYSTEM DC/DC APL5930KAI 51

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

VGA ADP3211MNR2G 82

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736RGRR 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

VGA G9661-25ADJF11U 83

INPUTS	OUTPUTS
3D3V_S0	1D8V_VGA_S0

VGA APL5930KAI 83

INPUTS	OUTPUTS
1D35V_S3	0D95V_VGA_S0

Switches 36,83

INPUTS	OUTPUTS
5V_S5 3D3V_S5 3D3V_S0	5V_S0 3D3V_S0 3D3V_VGA

VGA TPS51211DSCR

INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0 83

<Core Design>

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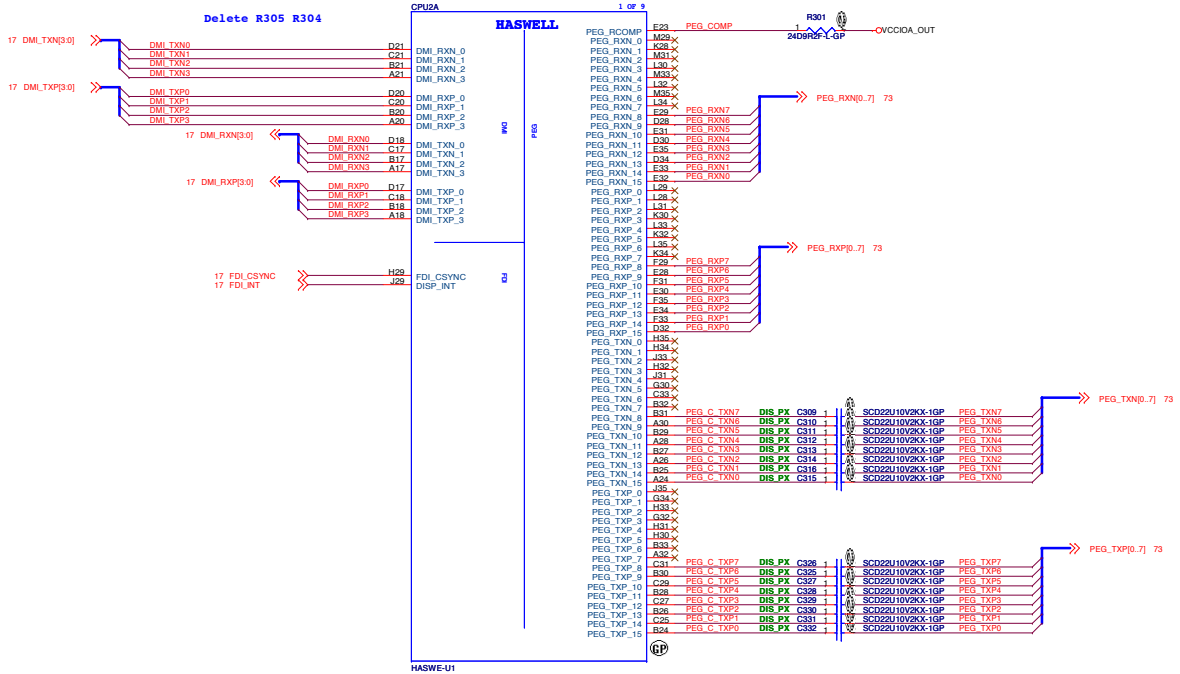
Title: **Block Diagram**

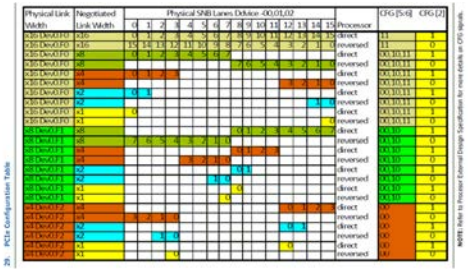
Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

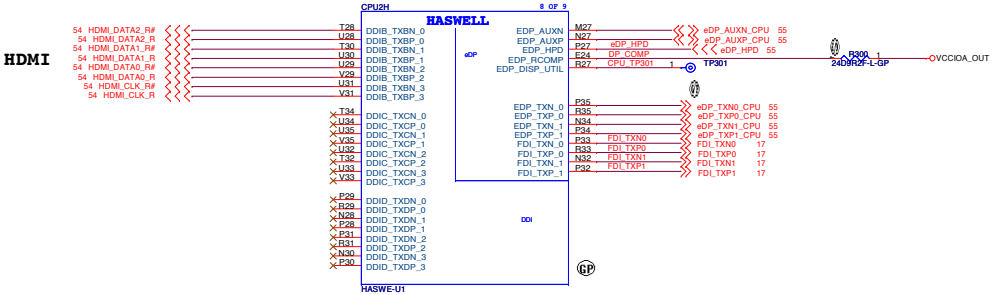
Date: Wednesday, July 03, 2013 Sheet 2 of 103

SSID = CPU

Delete R305 R304







<Core Design>

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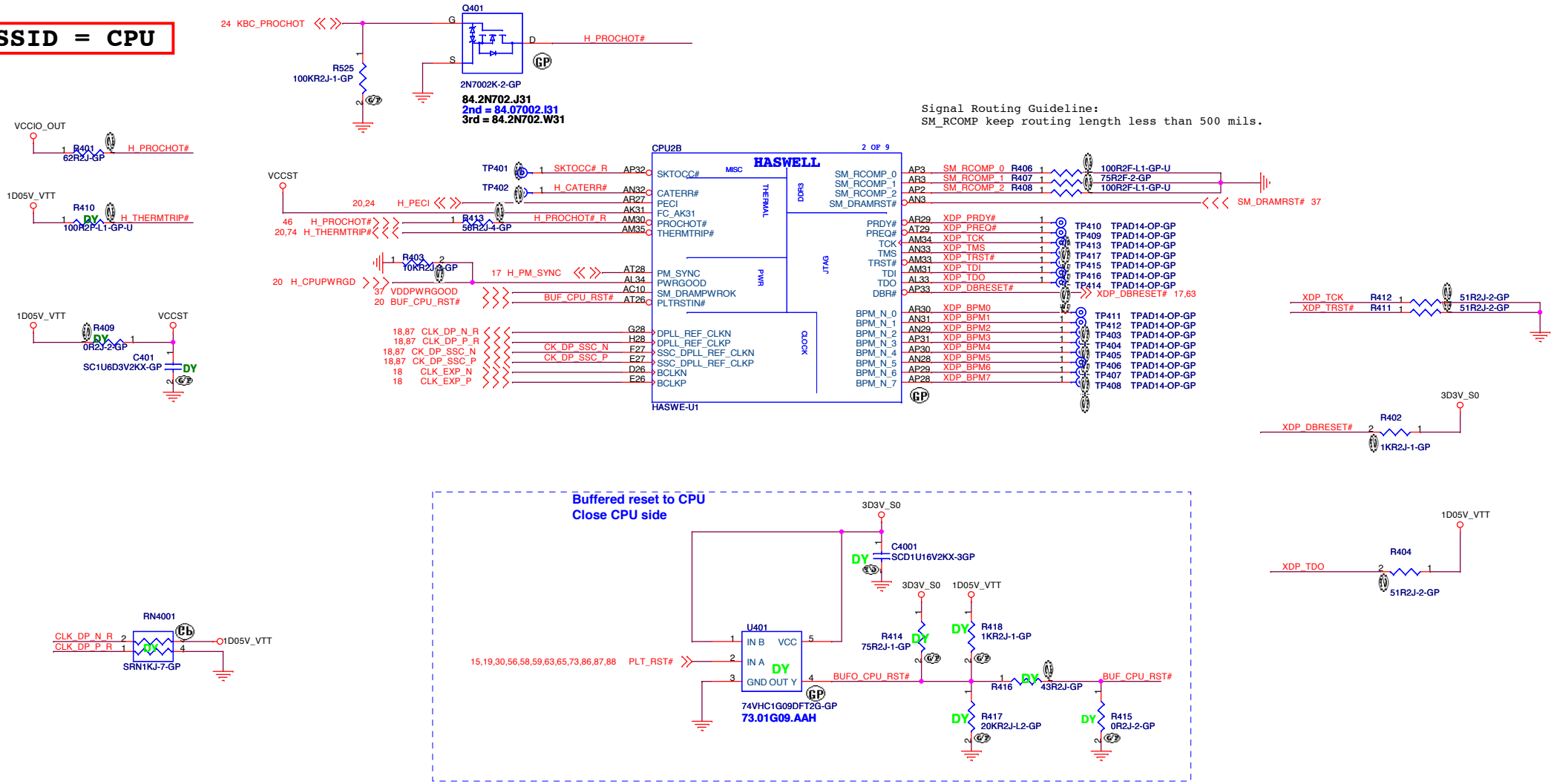
Title: CPU (PCIE/DMI/FDI)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 3 of 103

SSID = CPU

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



<Core Design>

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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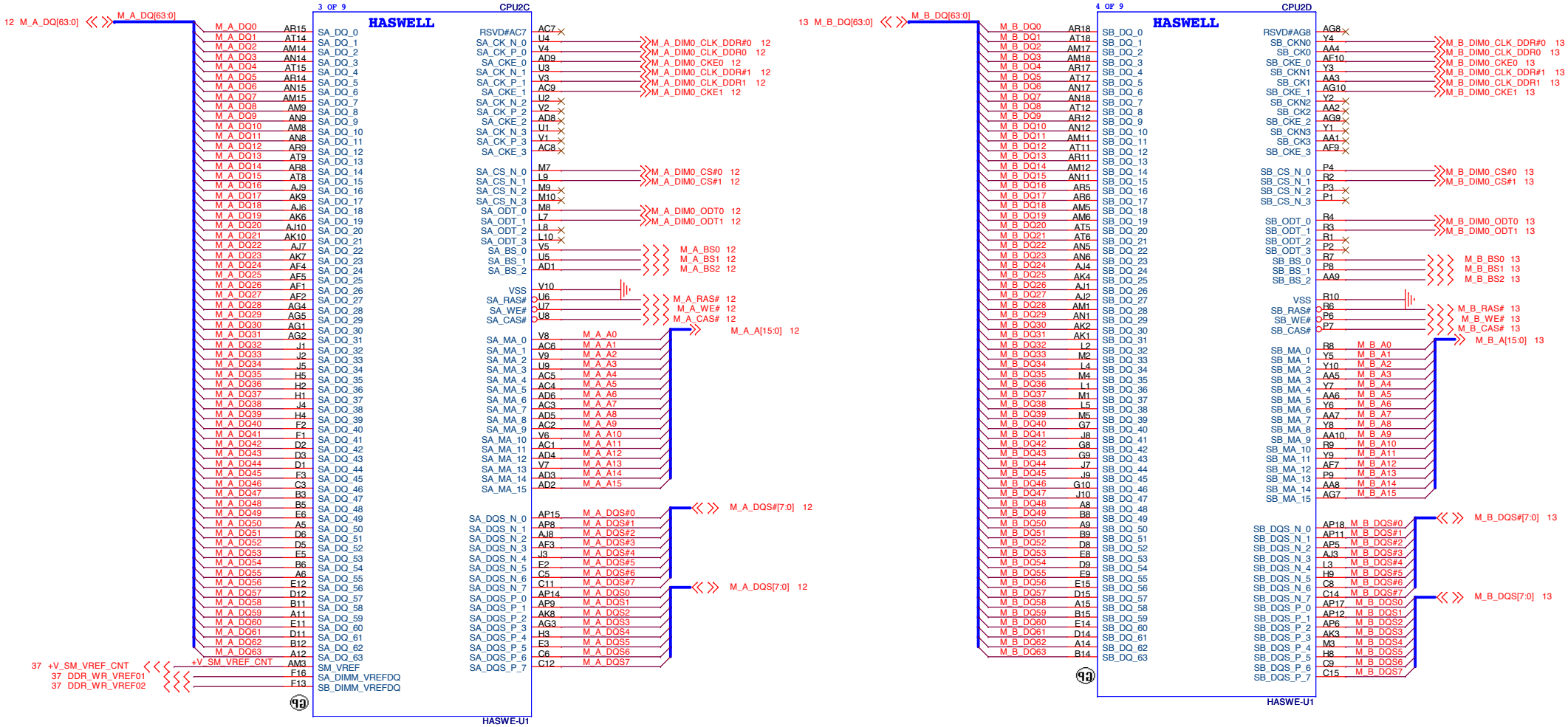
SSID = CPU



<Core Design>

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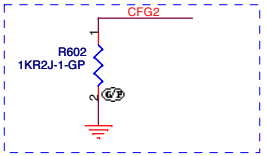
Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

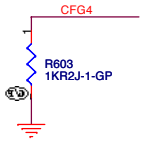
Date: Monday, August 12, 2013 Sheet 5 of 103

SSID = CPU

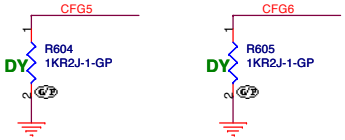
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



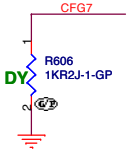
eDP Enable	
CFG4	1:Disable 0:Enable

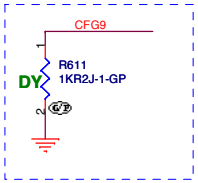


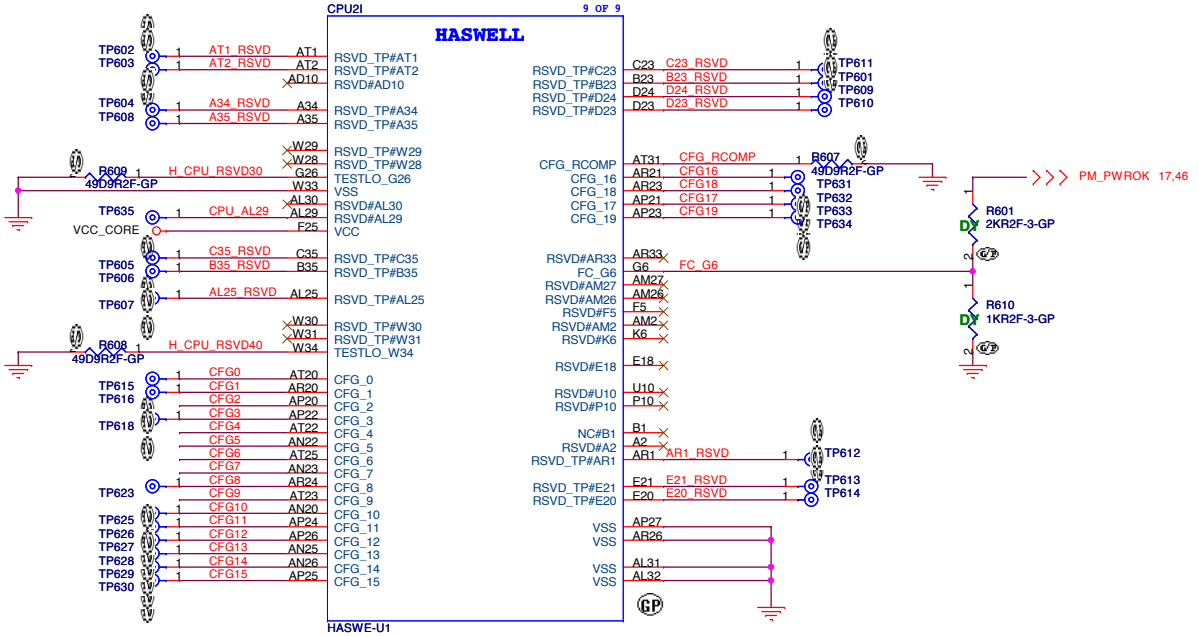
PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training







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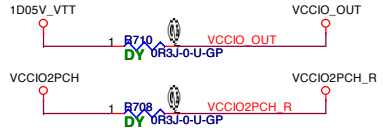
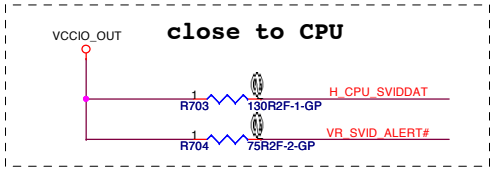
Title: **CPU (RESERVED)**

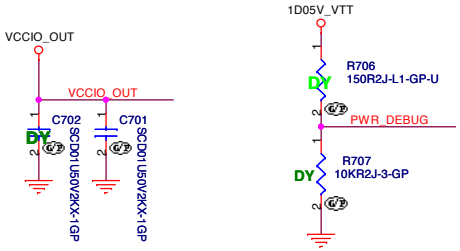
Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

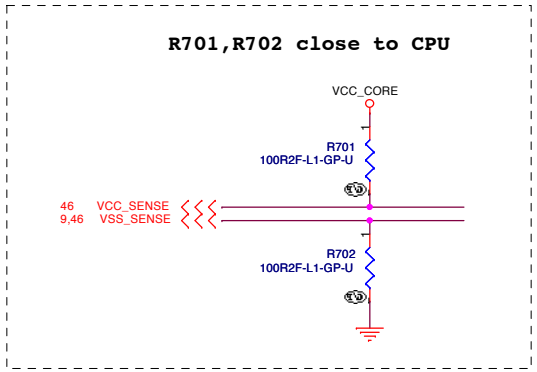
Date: Monday, August 12, 2013 Sheet 6 of 103

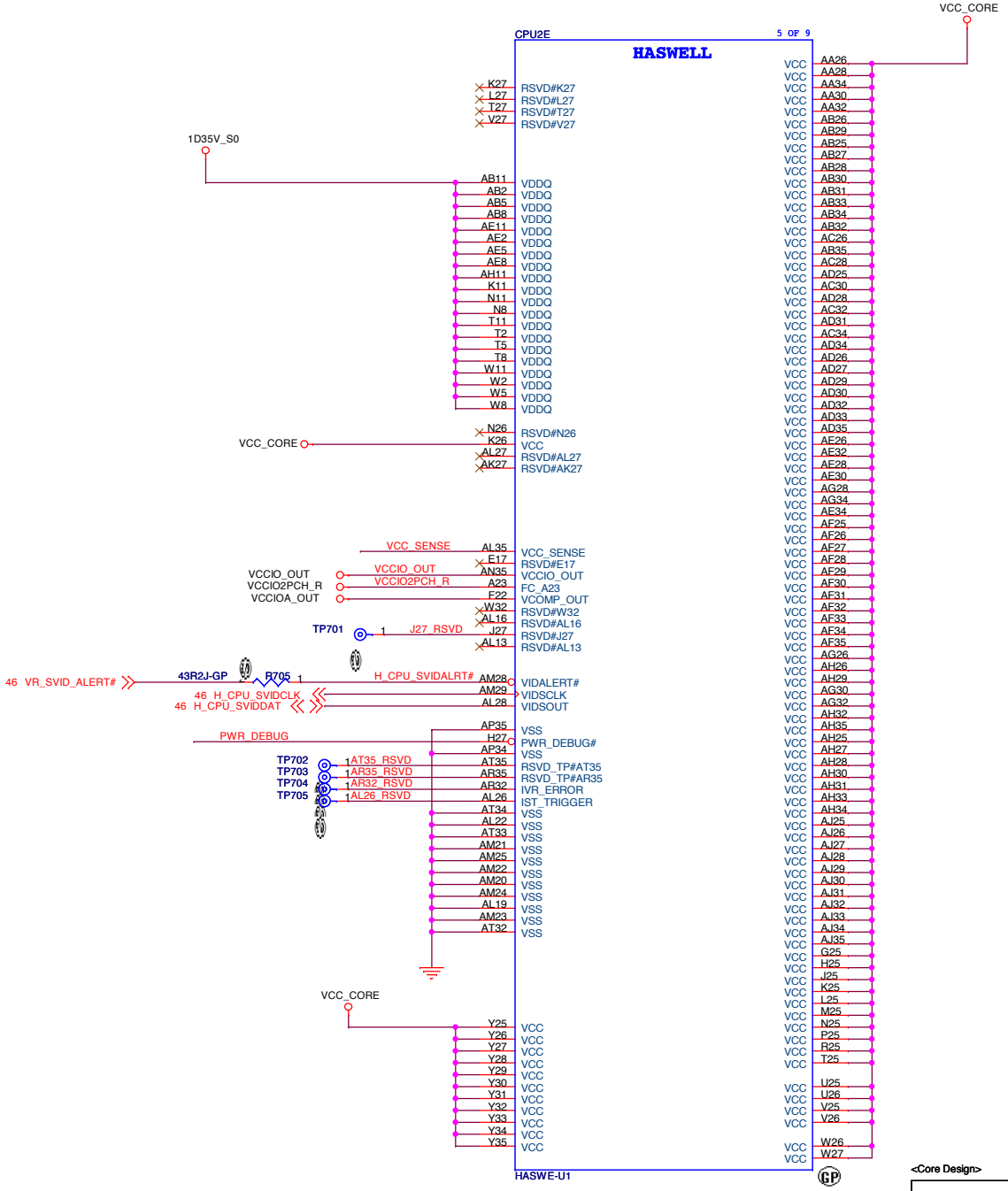
SSID = CPU











<Core Design>

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Title: CPU (VCC)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 7 of 103

(Reserved)

<Core Design>

緯創資通 Wistron Corporation
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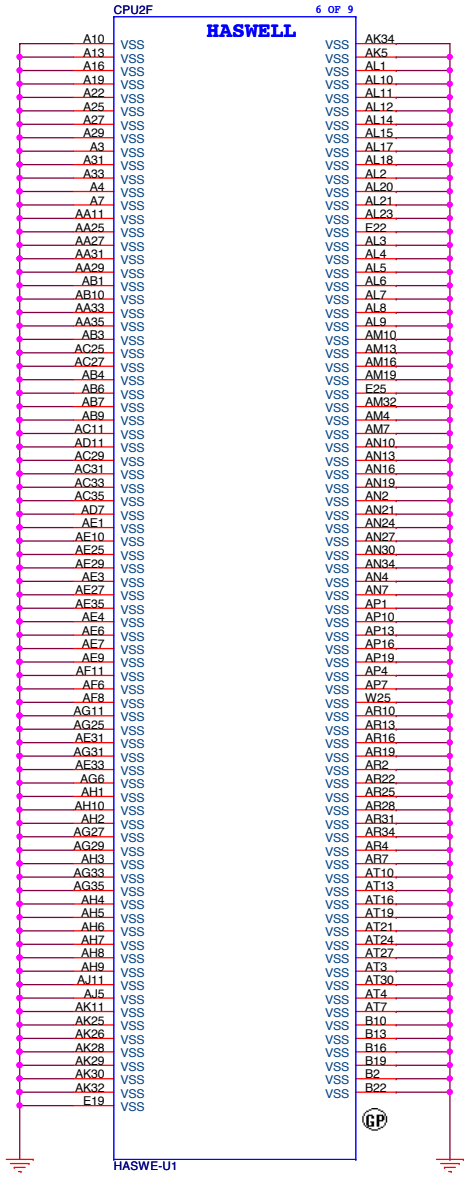
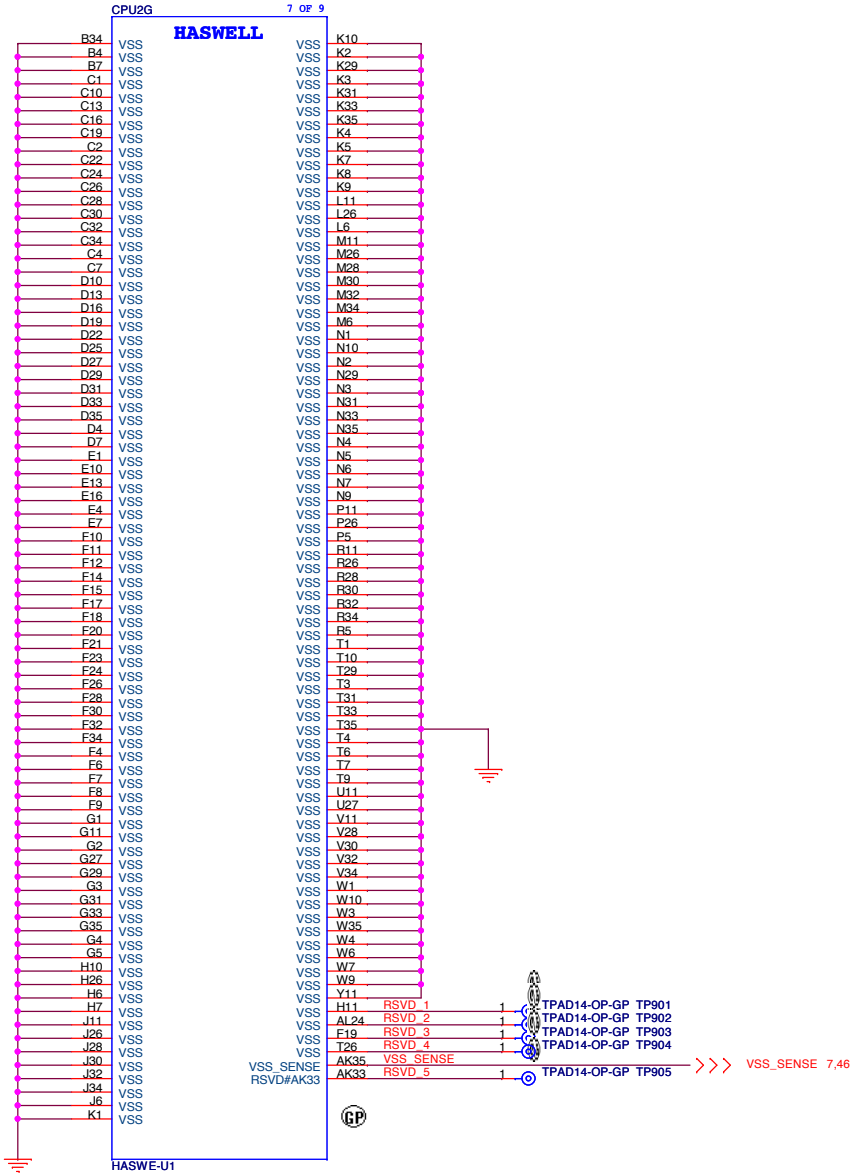
Title: CPU (DDI/EDP)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 8 of 103

SSID = CPU





<Core Design>

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Title: CPU (VSS)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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VCC_CORE

VCC_CORE
22uF x 19
10uF x 11

C1001 C1002 C1003 C1004 C1005 C1006 C1007 C1008 C1009 C1010
SC22U6D3V5MX-2GP

C1011 C1012 C1013 C1014 C1015 C1016 C1017 C1018 C1019
SC22U6D3V5MX-2GP

C1020 C1021 C1022 C1023 C1024 C1025 C1026 C1027 C1028 C1029 C1030
SC22U6D3V5MX-2GP

1D35V_S0

VCCDDQ
22uF x 11
10uF x 10
330uF x 1

C1031 C1032 C1033 C1034 C1035 C1036 C1037 C1038 C1039 C1040 C1041
SC22U6D3V5MX-2GP

C1042 C1043 C1044 C1045 C1046 C1047 C1048 C1049 C1050 C1051
SC10U6D3V3MX-GP

PC1001
SE330U2VDM-L-GP

79.33719.L01
2nd = 77.53371.21L

<Core Design>

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Title: ***010_CPU (Power CAP1)***

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 10 of 103

(Reserved)

<Core Design>

緯創資通 Wistron Corporation
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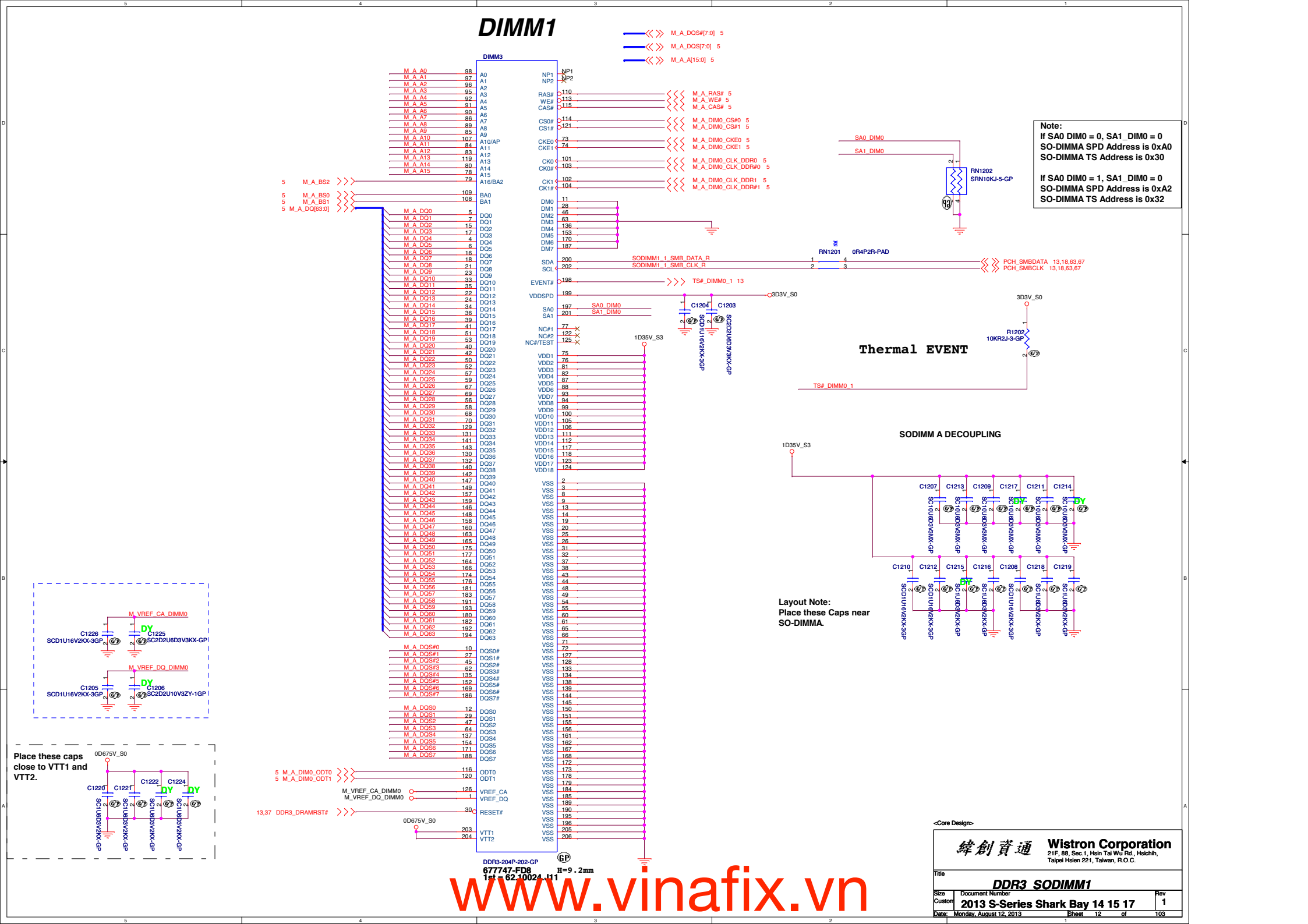
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(Power CAP2)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Wednesday, July 03, 2013 | Sheet 11 of 103

DIMM1



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

Place these caps close to VTT1 and VTT2.

<Core Design>

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Title: **DDR3_SODIMM1**

Size	Document Number	Rev
Custom	2013 S-Series Shark Bay 14 15 17	1

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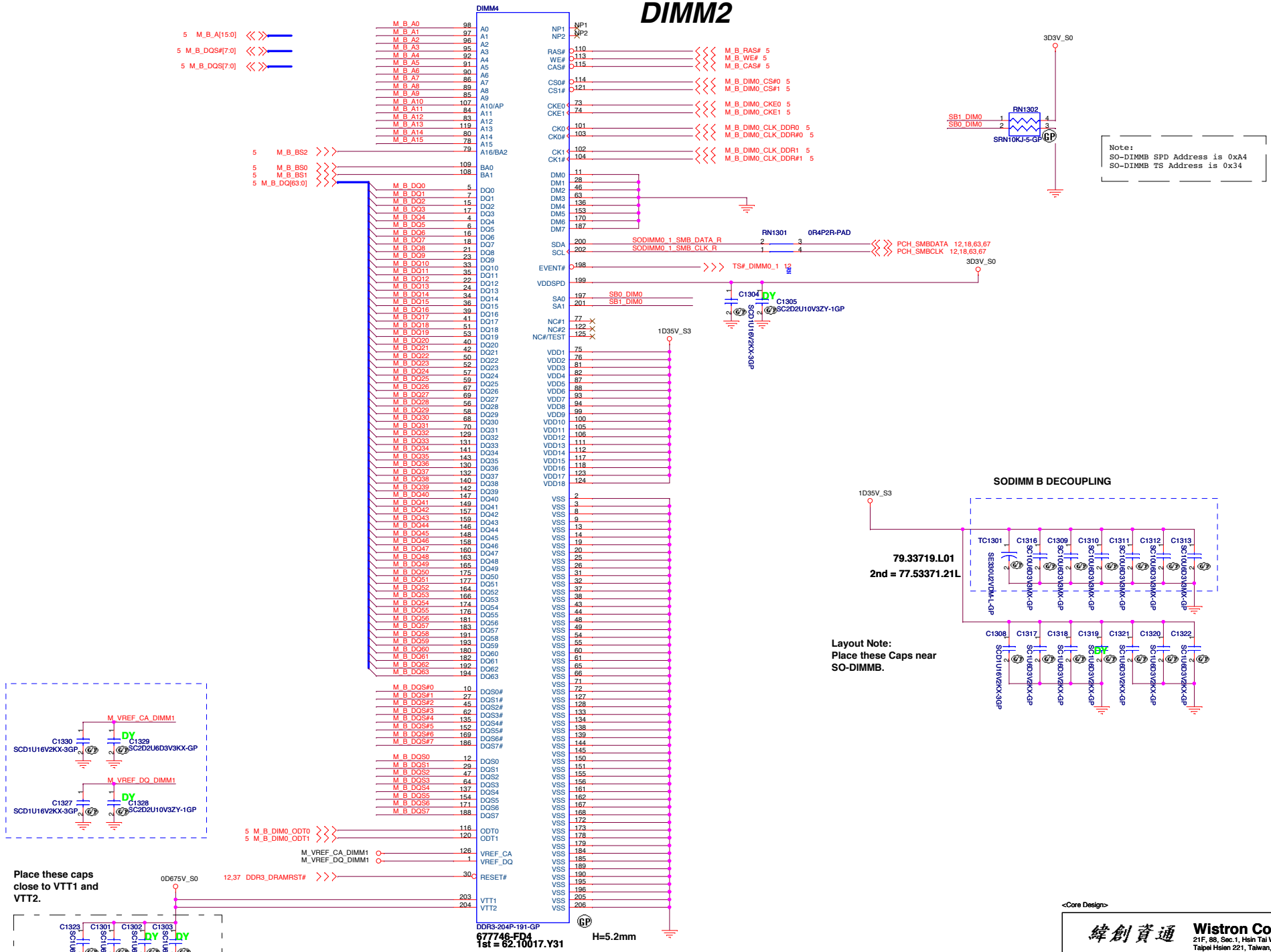
DIMM2



<Core Design>

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Title: DDR3 SODIMM2

Size	Document Number	Rev
Custom	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 13 of 103

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Title: (Reserved)SODIMM3

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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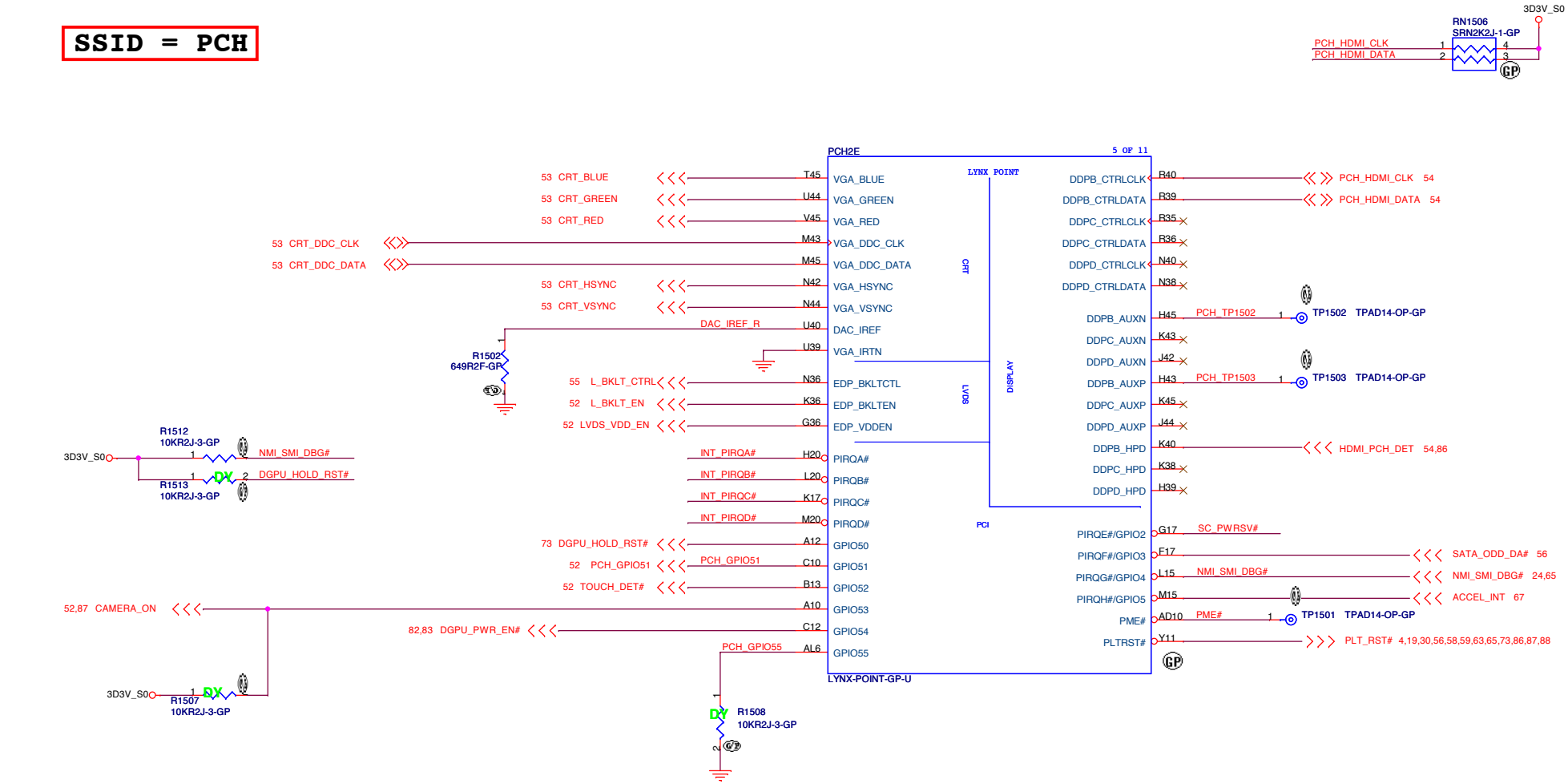
SSID = PCH



BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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Title: PCH (PCI/CRT/DDI)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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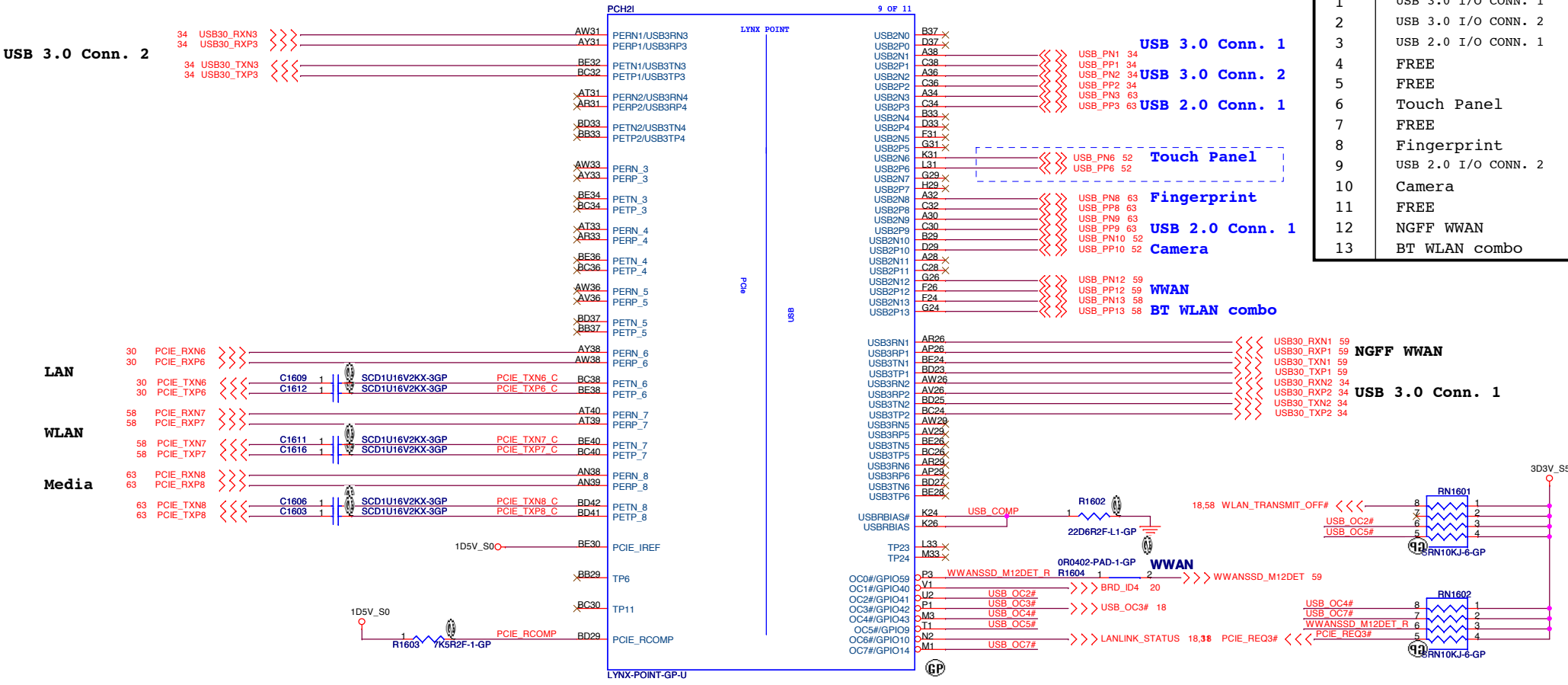
SSID = PCH

USB2.0 Table

USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 2.0 I/O CONN. 1
4	FREE
5	FREE
6	Touch Panel
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 2
10	Camera
11	FREE
12	NGFF WWAN
13	BT WLAN combo



<Core Design>

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Title: **PCH (PCIE/USB)**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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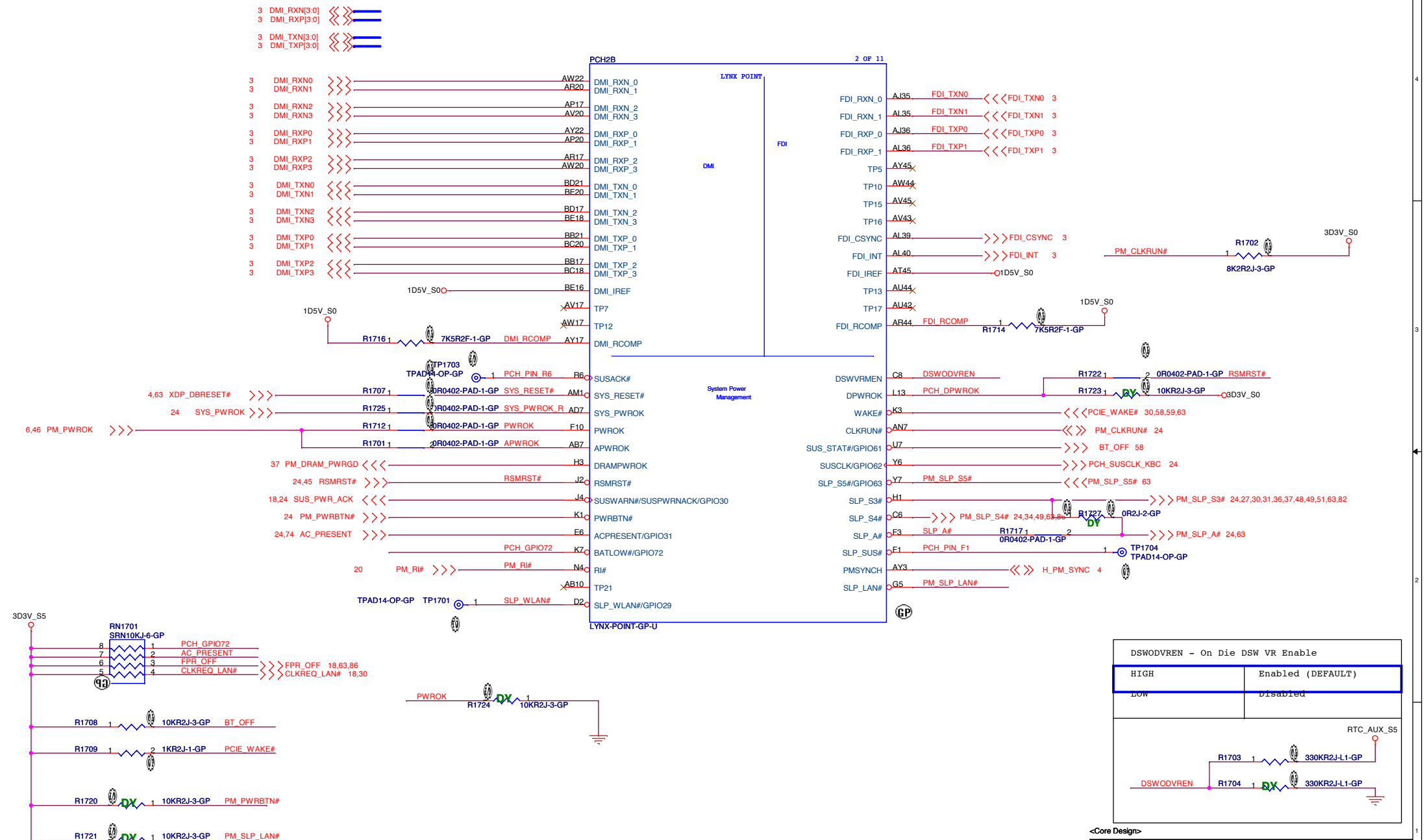
SSID = PCH



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (DMI/FDI/PM)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 17 of 103

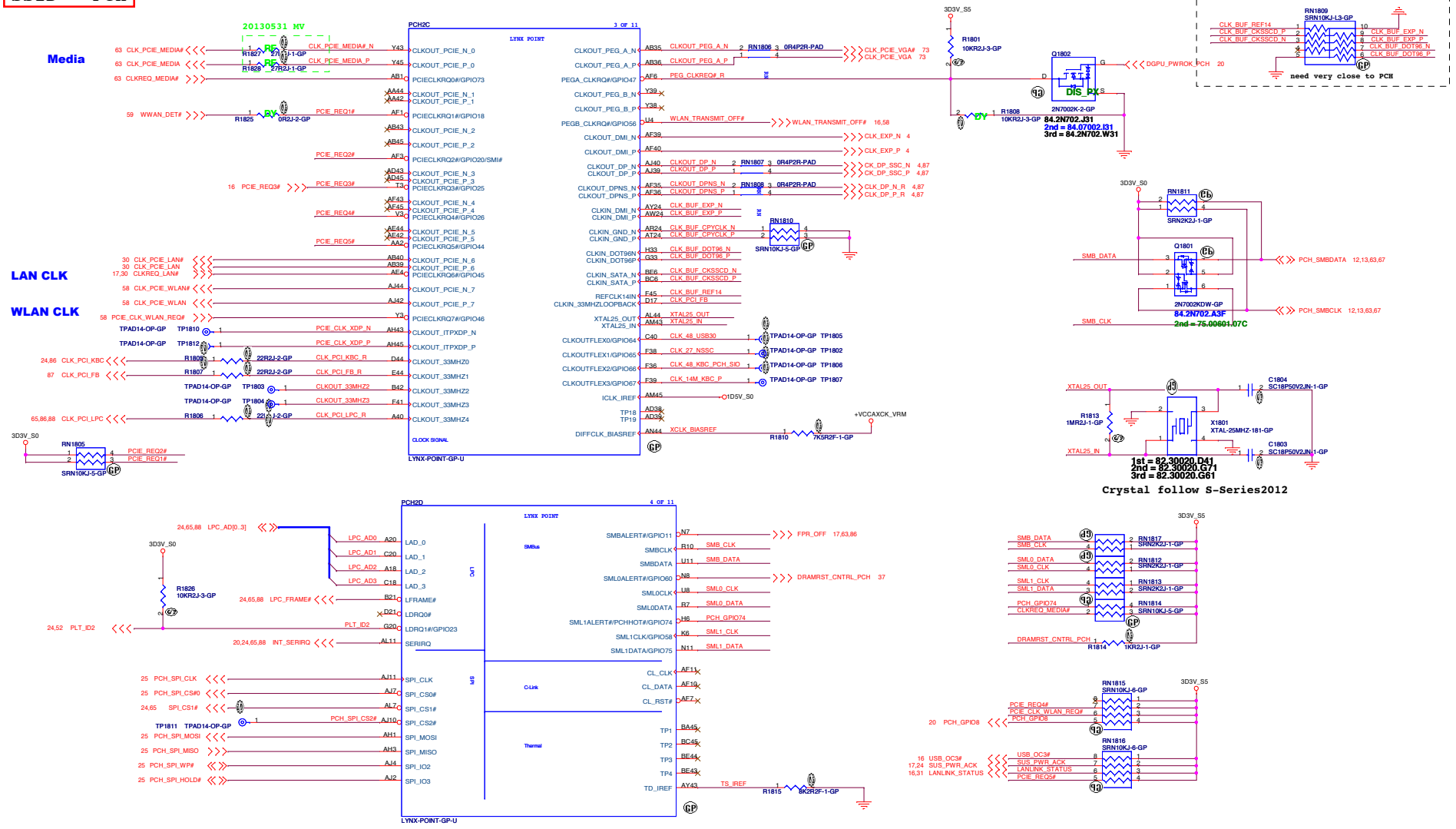
SSID = PCH

20130531 MV

Media

LAN CLK

WLAN CLK



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Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 18 of 103

SSID = PCH

Close to PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

HDA_SYNC:
HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap
is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase.

<Core Design>
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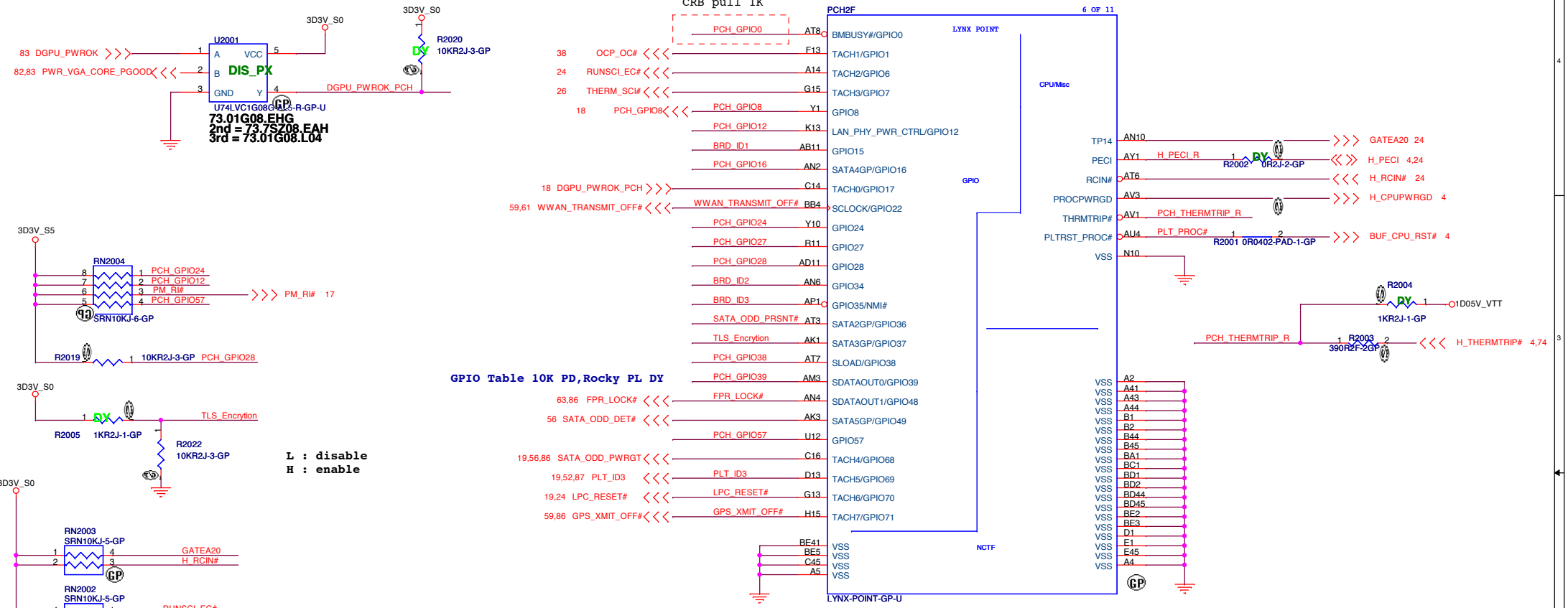
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (RTC/SATA/HDA/JTAG)
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1
Date: Monday, August 12, 2013 | Sheet 19 of 103

SSID = PCH



VBIOS ID TABLE

PCH_GPIO39	PCH_GPIO38	
0	1	128MX16
1	0	N/A
1	1	UMA
0	0	64MX16

	GPIO23 PLT_ID2	GPIO69 PLT_ID3
Rampage 14"	0	1
Renegade 15"	1	0
Racquet 17"	1	1

	BRD_ID1 GPIO15	BRD_ID2 GPIO34	BRD_ID3 GPIO35	BRD_ID4 GPIO40
DB 0	0	0	0	0
DB 1	0	0	0	1
DB 2	0	0	1	0
	0	0	1	1
SI 1	0	1	0	0
SI 1B	0	1	0	1
SI 2	0	1	1	0
	0	1	1	1
PV 1	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
MV	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

<Core Design>

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Title: PCH (GPIO/CPU)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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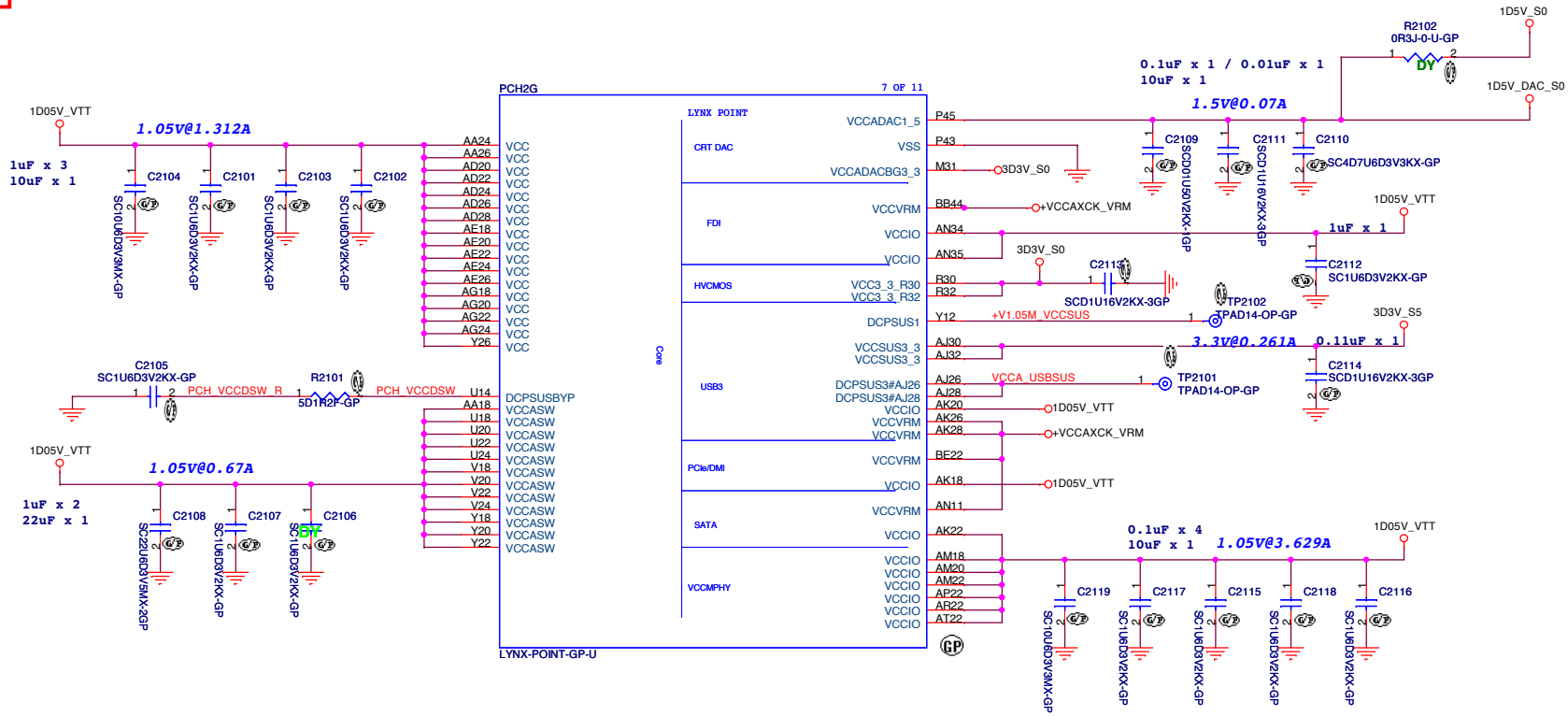
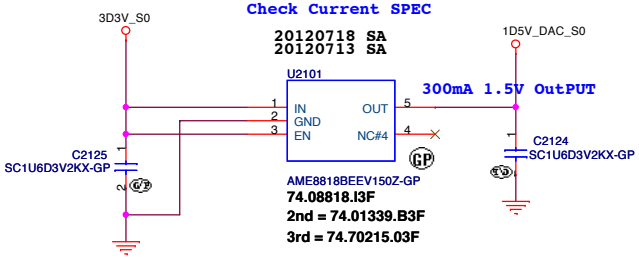
SSID = PCH





<Core Design>

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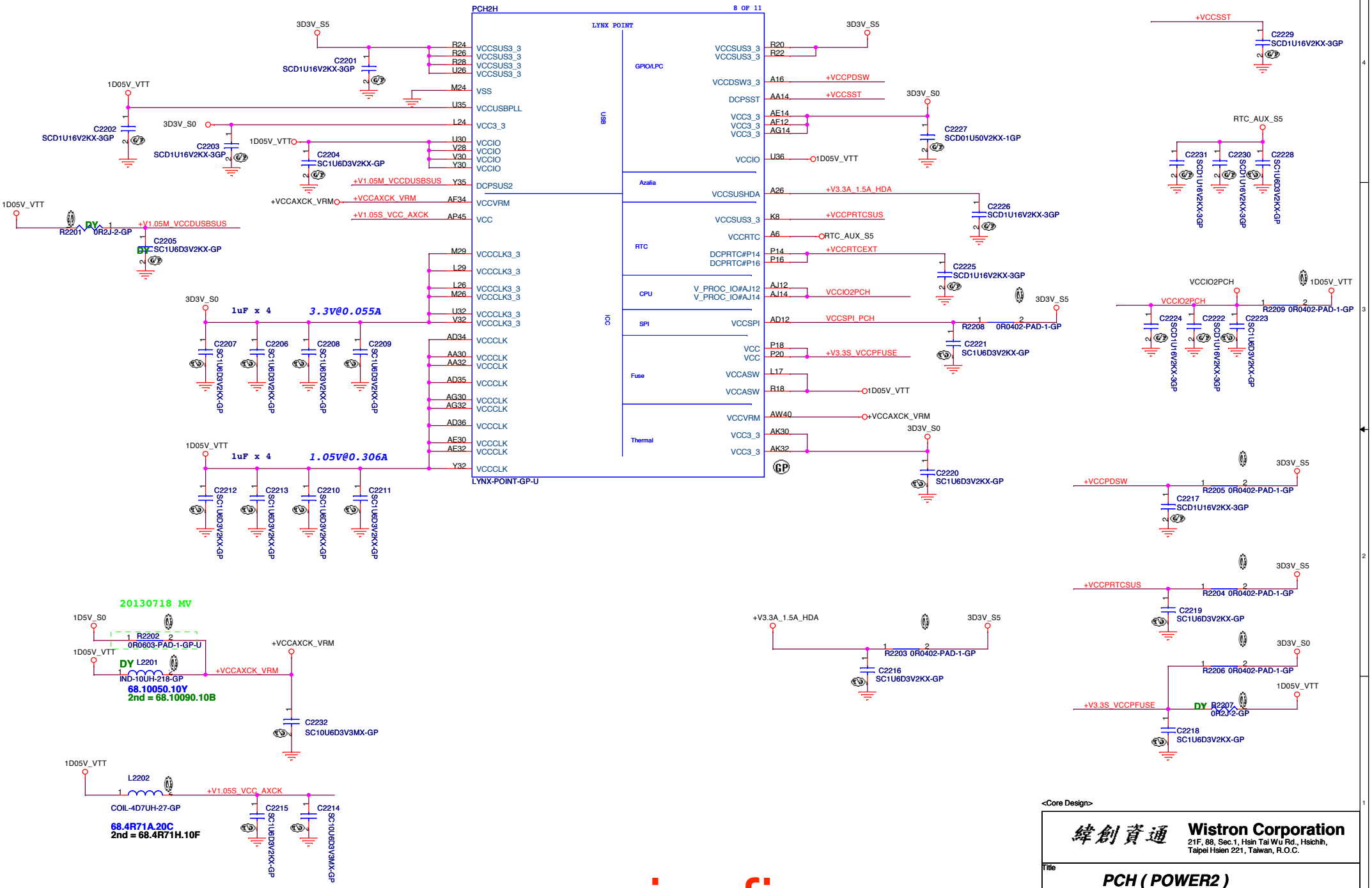
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

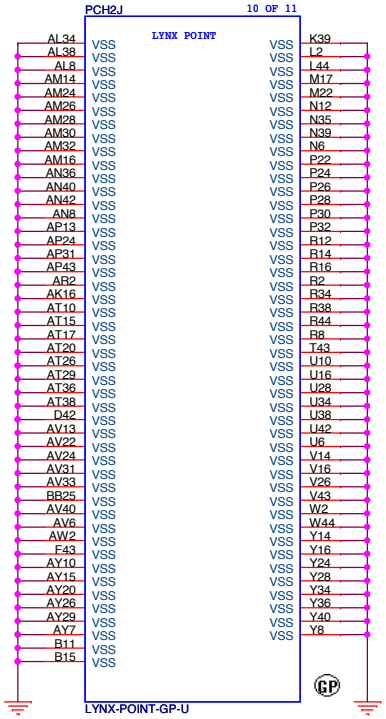
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

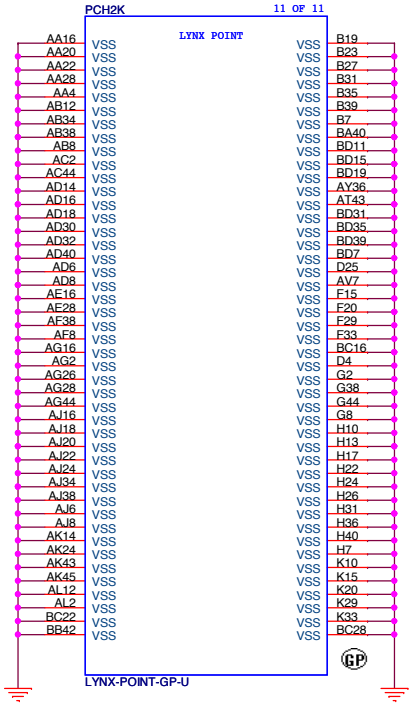
Date: Wednesday, July 24, 2013 | Sheet 21 of 103

SSID = PCH



SSID = PCH





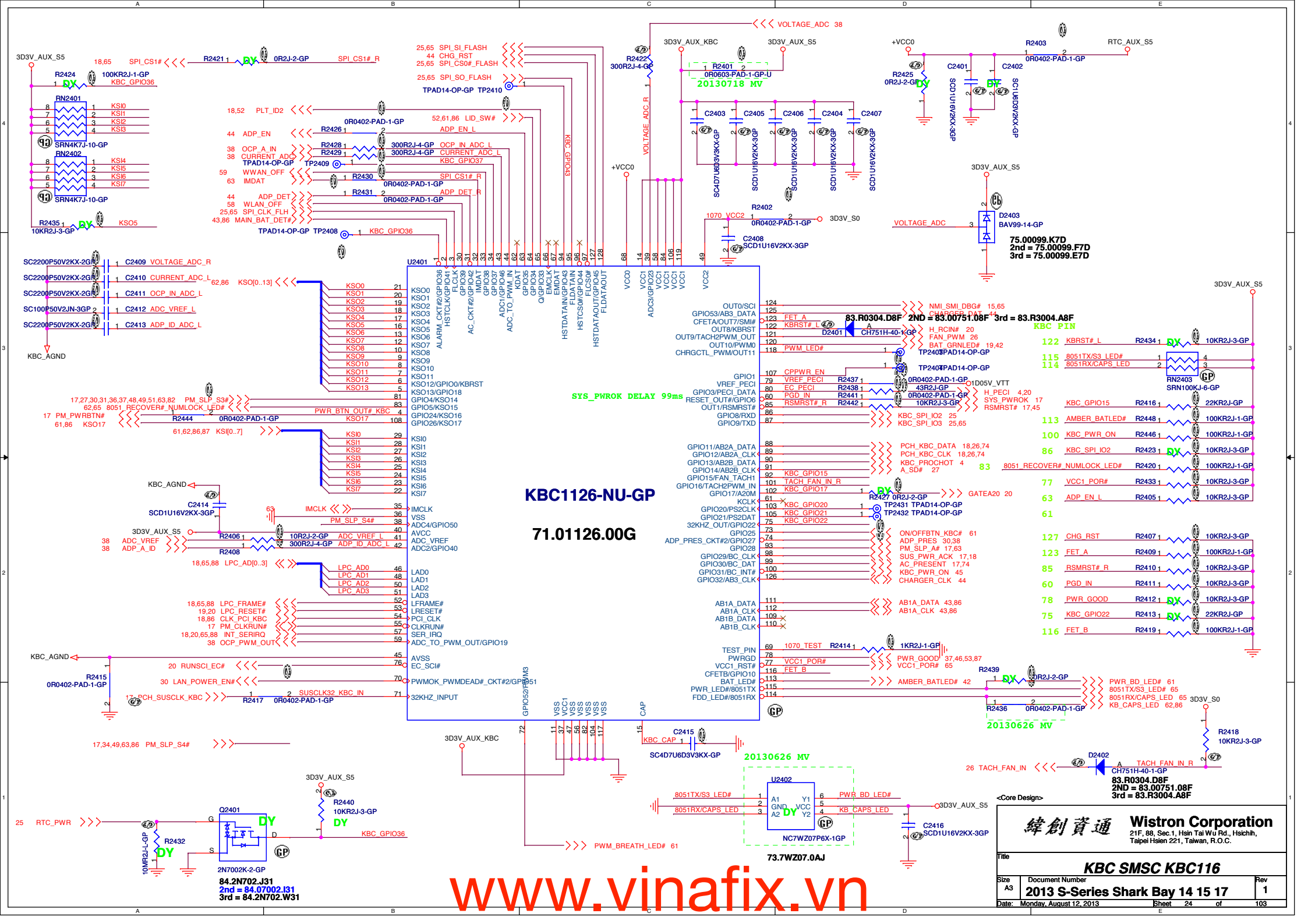
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH(VSS)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 23 of 103



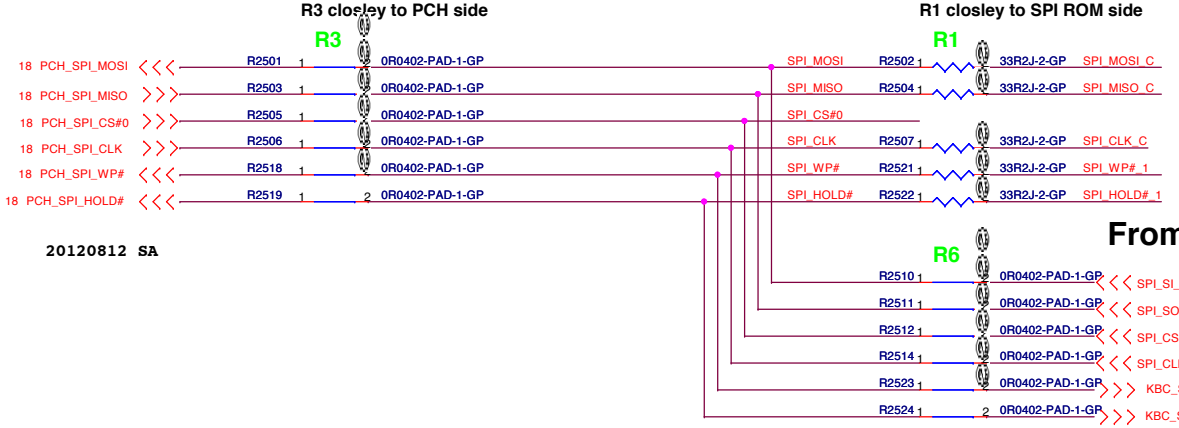
SPI FLASH ROM (8M byte) for PCH

To PCH

From BIOS

R3 closley to PCH side

R1 closley to SPI ROM side

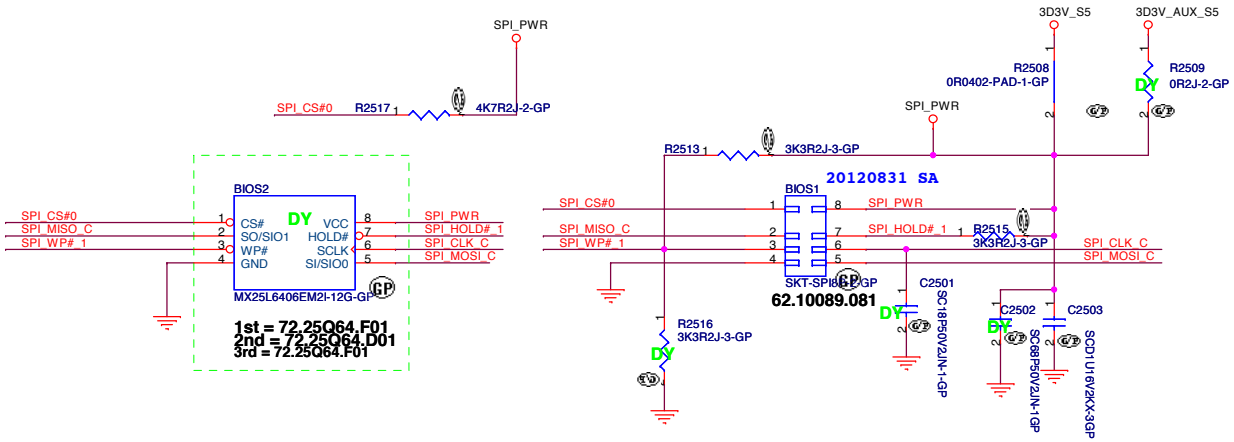


20120812 SA

From KBC

SPI_CLK SPI_CLK 87 To RF CAP

SYSTEM SPI ROM Socket

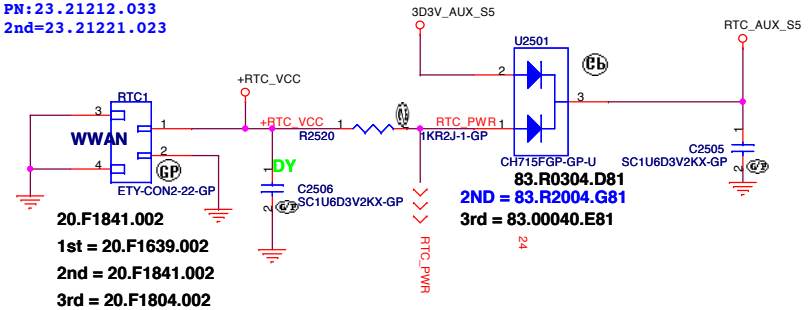


NOTE: SPI signal use GND reference

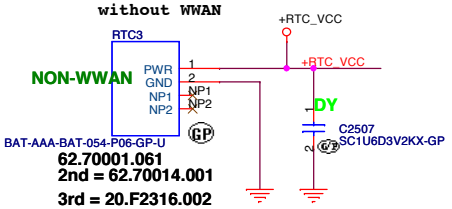
Quad IO Winbond 8M:72.25Q64.K01 (W25Q64FVSSIQ)
MXIC : 72.25647.00A (MX25L6473EM2I)
Micon: 72.25Q64.G01 (N25Q064A13ESEC0F)

RTC Battery

RTC Battery+Cable
PN:23.21212.033
2nd=23.21221.023



without WWAN



RTC Battery PN:23.22065.001
23.22063.001
23.20068.001

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

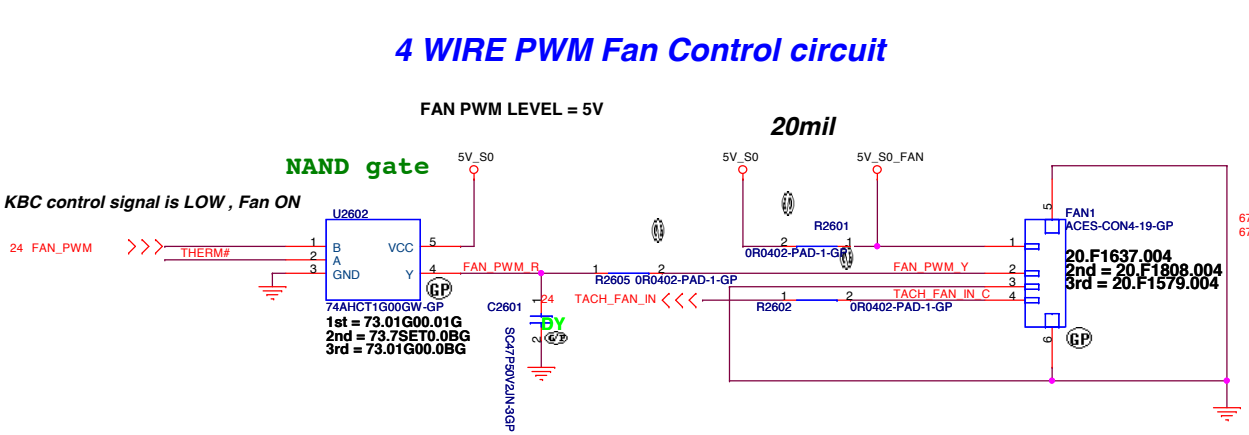
Title: Flash(KBC+PCH)/RTC

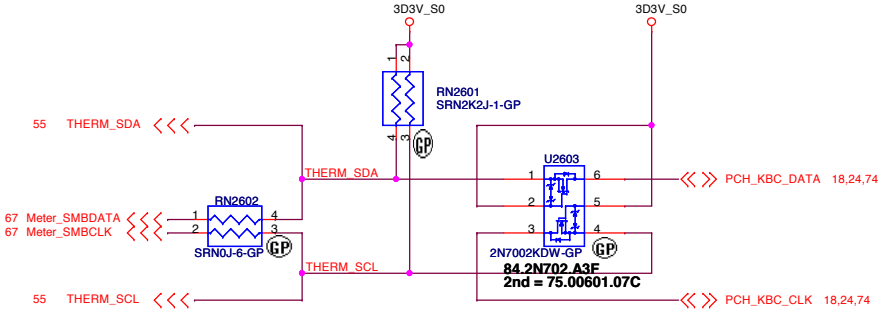
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 25 of 103

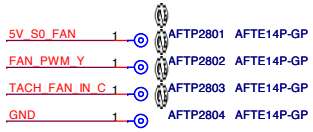
Thermal Sensor,FAN

4 WIRE PWM Fan Control circuit

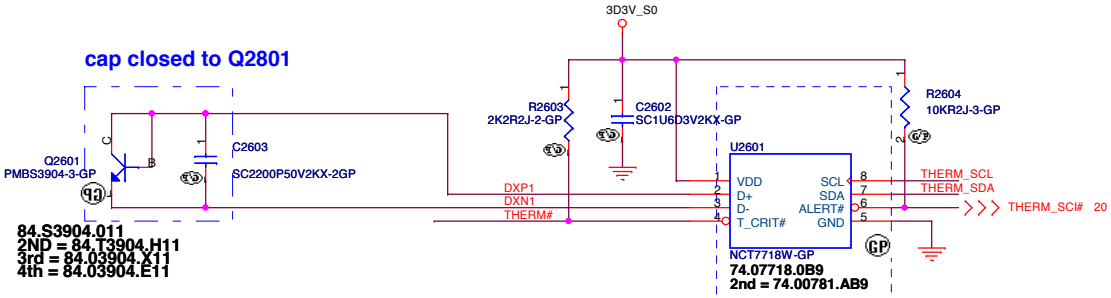




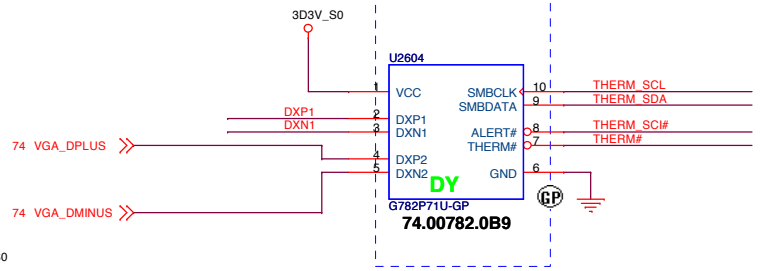
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L



Thermal IC Control circuit

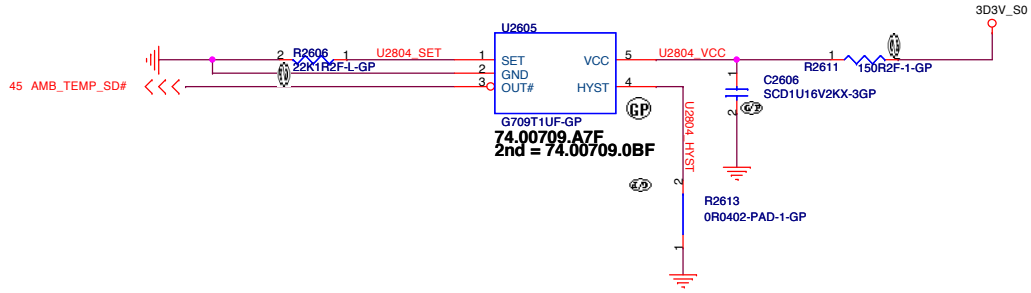


Co-Layout

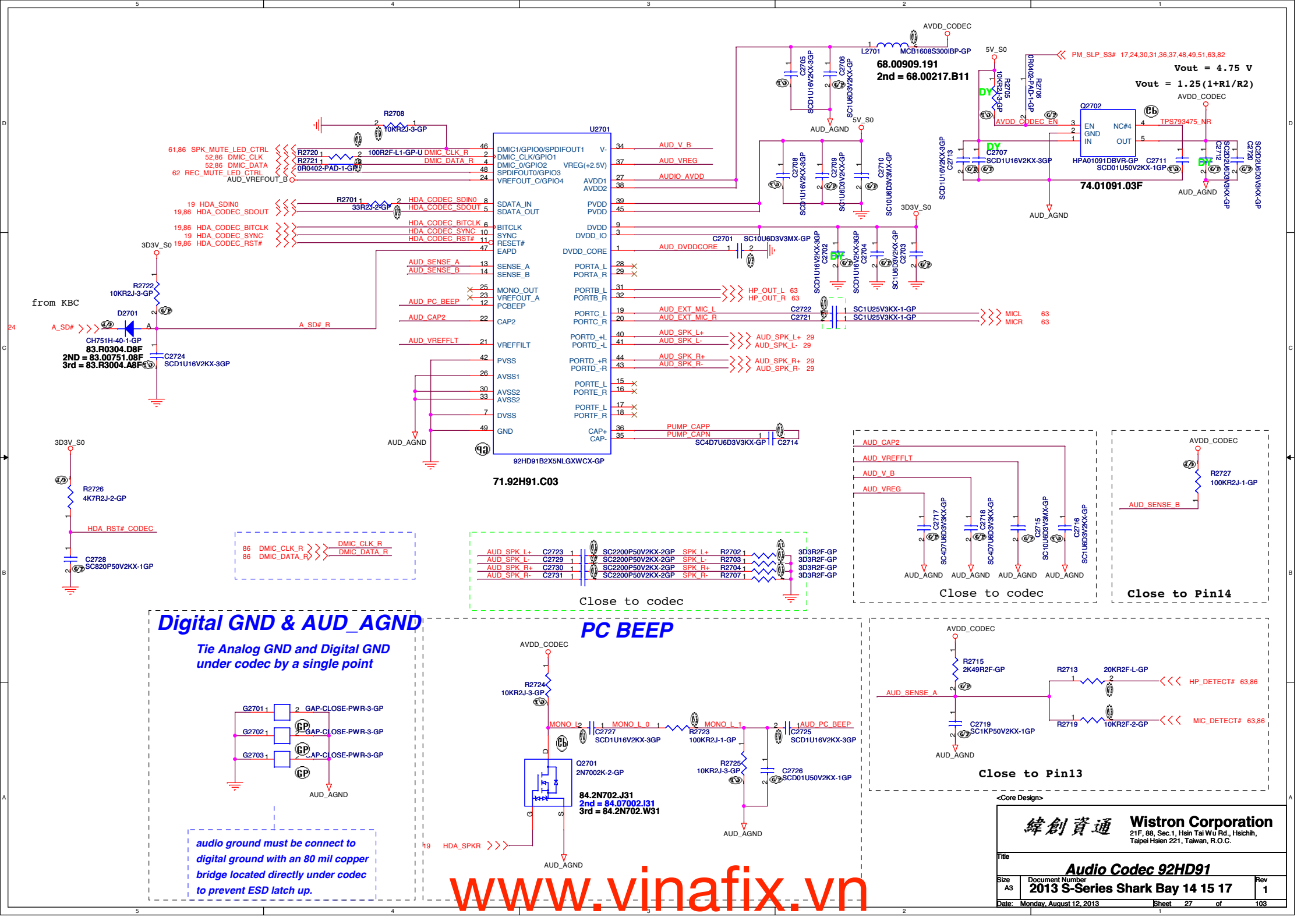


T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: Thermal G781/Fan control
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1
Date: Monday, August 12, 2013 | Sheet 26 of 103


AVDD_CODEC
L2701 MCB1608S300IBP-GP
68.00909.191
2nd = 68.00217.B11
5V_S0
PM_SLP_S3# 17,24,30,31,36,37,48,49,51,63,82
Vout = 4.75 V
Vout = 1.25(1+R1/R2)
Q2702
HPA01091DBVR-GP
TPS793475_NR
74.01091.03F
AUD_AGND
3D3V_S0
U2701
92HD91B2X5NLGXWCX-GP
71.92H91.C03
from KBC
D2701
CH751H-40-1-GP
83.R0304.D8F
2ND = 83.00751.08F
3rd = 83.R3004.A8F
A_SD#
A_SD#_R
HDA_RST#_CODEC
DMIC_CLK_R
DMIC_DATA_R
Close to codec
Close to Pin14
Close to Pin13
Digital GND & AUD_AGND
Tie Analog GND and Digital GND under codec by a single point
audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.
PC BEEP
Q2701
2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
HDA_SPKR
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec 92HD91
2013 S-Series Shark Bay 14 15 17
Monday, August 12, 2013
www.vinafix.vn

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO AMP(Reserved)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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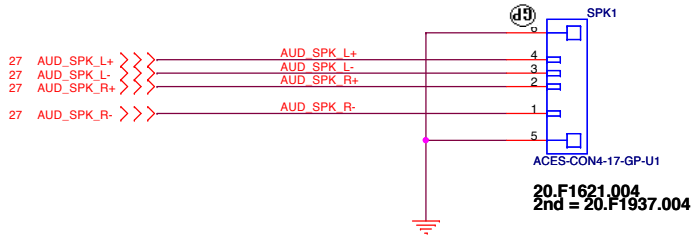
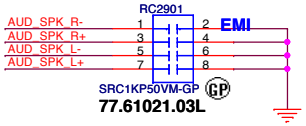
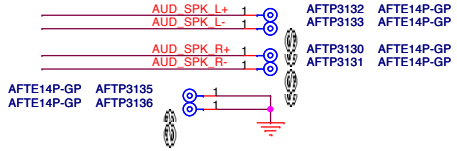
Speaker Connector







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 29 of 103

LAN RJ45

USE EFuse No ASF

DEL

LAN CHIP-RTL8151GH

C3026 to C3012

40 mils (average 100mA)

3D3V_LAN_S5

C3024 SCD1U16V2KX-3GP
C3022 SCD1U16V2KX-3GP
C3009 SCD1U16V2KX-3GP
VDDREG
Remove R3003
C3012 SC4D7U6D3V3KX-GP
C3016 SCD1U16V2KX-3GP
C3017 SCD1U16V2KX-3GP

C3001 to C3017

LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS

cap near pin11,32 <200mils

Regout power plane(1D05V)

VDD10

cap near pin3,8,22,30

C3023 SCD1U16V2KX-3GP
C3020 SCD1U16V2KX-3GP
C3007 SCD1U16V2KX-3GP
C3021 SCD1U16V2KX-3GP

60 mils (average 300mA)

20130718 MV

REGOUT
R3007 0R0603-PAD-1-GP-U
20130805 MV

C3008 SC1U6D3V2KX-GP
C3014 SC4D7U6D3V3KX-GP
C3015 SCD1U16V2KX-3GP
C3013 SC1U6D3V2KX-GP

Put 4D7U L + 4D7U cap near pin24 <200mils
(2nd = 78.22610.81L)

3D3V_LAN_S5

R3006 4K02R2F-GP
PCIE_WAKE# 17,58,59,63
PCIE_WAKE#_LAN_B
Q3002 PMBS3904-3-GP
R3008 2KR2J-1-GP
R3009 0R2J-2-GP
PCIE_WAKE#_LAN

84.S3904.011
2nd = 84.T3904.H11
3rd = 84.03904.X11
4th = 84.03904.E11

EEPROM LED OPTION USE '00'
=> LED0 : ACT (Amber)
=> LED1 : LINK (White)
(BOTH 10/100 & GIGA CHIP)
(Power down => Kept high)

R3004 2K49R2F-GP
RSET
YELLOW_LED# 31,86
GREEN_LED# 31,86
LAN_LED3#
TP3001 TPAD14-OP-GP

U3001
GND
AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED1/GPO LED2
3D3V_LAN_S5 VDD10 LANXOUT LANXIN

MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3
VDD10
AVDD10 AVDD33 CLKREQB HSIP HSIN REFCLK_P REFCLK_N
REGOUT VDDREG DVDD10 LANWAKE# ISOLATE# PERST# HSON HSOP
PCIE_WAKE#_LAN
PCIE_RXN6_R
PCIE_RXP6_R
C3011 SCD1U16V2KX-3GP
C3010 SCD1U16V2KX-3GP
PLT_RST# 4,15,19,56,58,59,63,65,73,86,87,88
PCIE_RXN6 16
PCIE_RXP6 16

RTL8151GH-CGT-GP-U1
71.08151.M05

CLK_PCIE_LAN# 18
CLK_PCIE_LAN 18
PCIE_TXN6 16
PCIE_TXP6 16
CLKREQ_LAN# 17,18
3D3V_LAN_S5

DB	RTL8151GH
SI	RTL8151GH

RTL8161GSH
Install:L3003 C3030 C3031 C3026 C3001
DY:R3007

Lan Power Inductance Spec
(1) IDC >= 600mA
(2) Tolerance < 20%
(3) RDC <= 0.8ohms(Max)
(4) Efficiency >= 80%

3D3V_LAN_S5 rise time controlled between 0.5mS and 100mS.

3D3V_S5

Q3001 DMP2305U-7-GP
84.02305.G31
2nd = 84.02377.031
3rd = 84.02305.I31
C3002 SC1U6D3V2KX-GP
R3001 100KR2J-1-GP
C3025 SCD1U16V2KX-3GP
LAN_POWER_EN#_R
R3002 10KR2F-2-GP
24 LAN_POWER_EN#
R3005 0R0402-PAD-1-GP
Q3004 2N7002KDW-GP
24,38 ADP_PRES
PM_SLP_S3# 17,24,27,31,36,37,48,49,51,63,82
LAN_POWER#
84.2N702.A3F
2nd = 75.00601.07C

Using Efuse
Without ASF

25MHz Crystal

C3004 SC15P50V2JN-2-GP
LANXOUT
XTAL-25MHZ-181-GP
X3001
1st = 82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61
Q3005
LANXIN 86

Isolate Strap Pin

3D3V_S0
R3011 1KR2J-1-GP
ISOLATE#
R3014 15KR2F-GP

<Core Design>

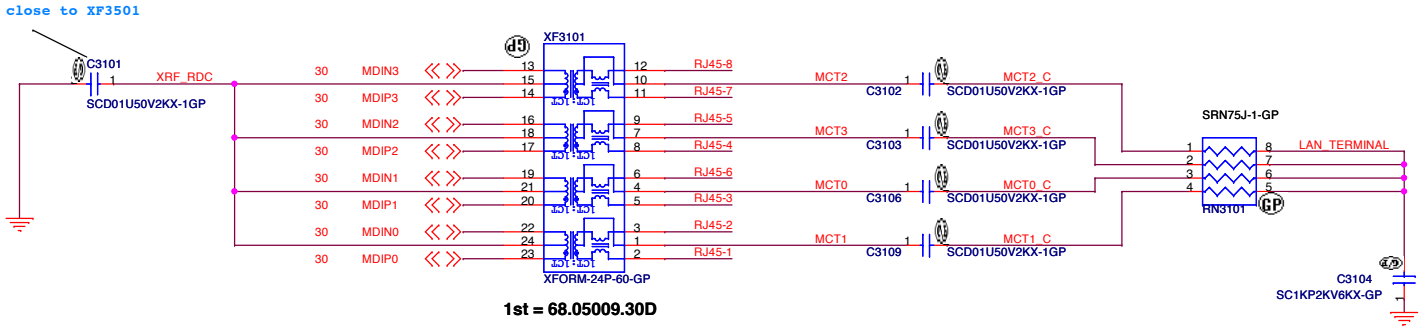
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Lan Realtek 8151GH

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

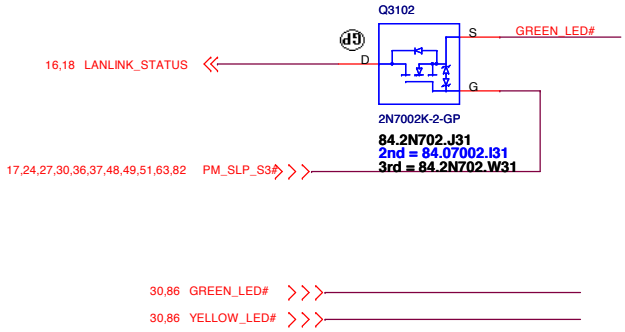
Date: Monday, August 12, 2013 Sheet 30 of 103

White LED for connectivity and Amber LED for activity located on RJ-45 connector



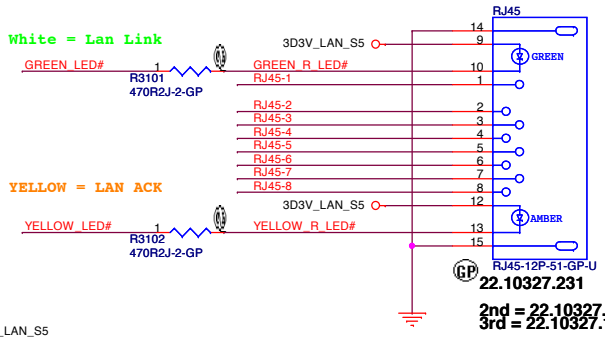
1st = 68.05009.30D
2nd = 68.89240.30D
3rd = 68.IH601.301

RJ45 Connector



84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

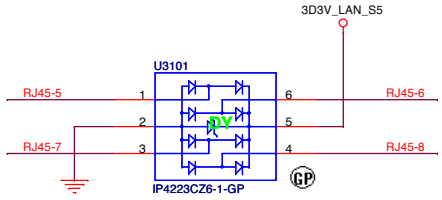
wavelength : Orange 605mm need check



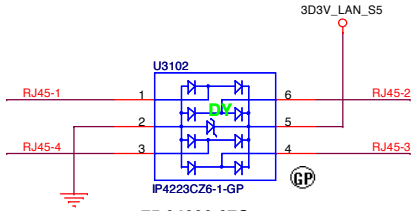
22.10327.231
2nd = 22.10327.151
3rd = 22.10327.171

Green
10(+),9(-)
YELLOW
12(+),13(-)

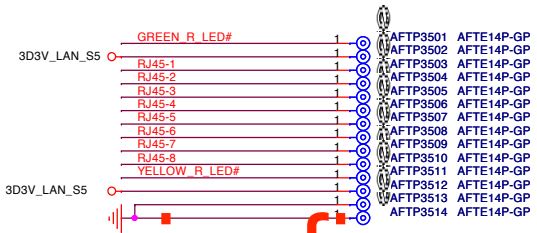
(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.



75.04223.07C
2nd = 75.09904.07C
3rd = 75.02304.07C



75.04223.07C
2nd = 75.09904.07C
3rd = 75.02304.07C



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45+Transformer

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 31 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Card Reader-JMB 709***

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 32 of 103

<Variant Name>

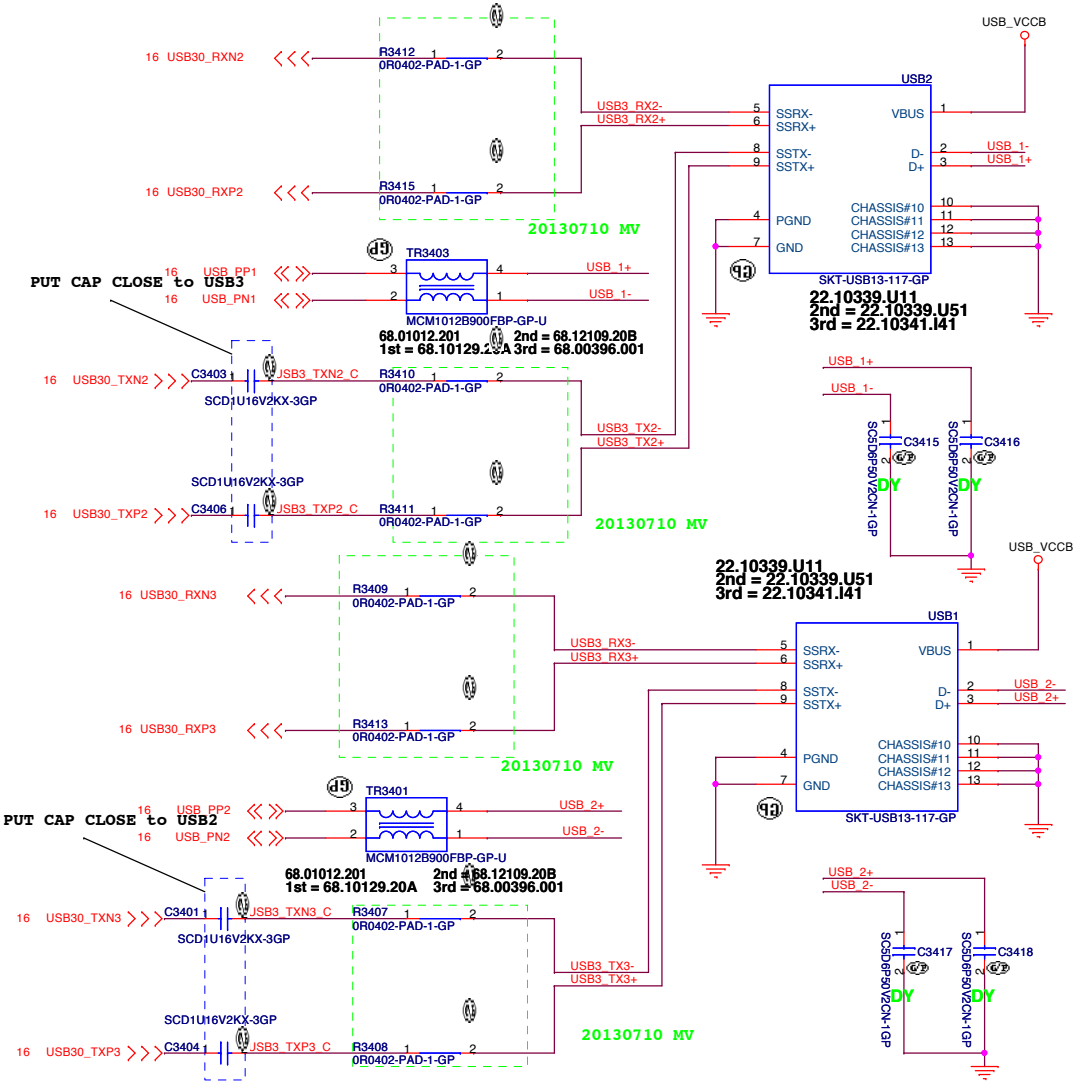
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CARD Reader CONN

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 33 of 103

Left Side USB 3.0 Connector

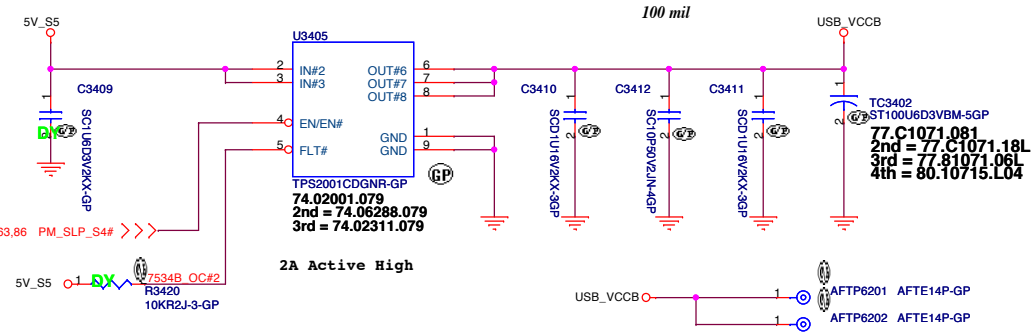


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

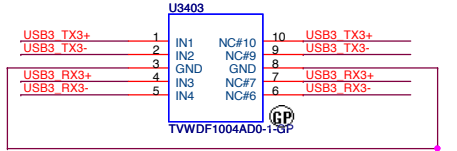
USB 3.0/2.0 Port Pairing

USB3.0	USB2.0
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3
Port 5	Port 4
Port 6	Port 5

USB POWER

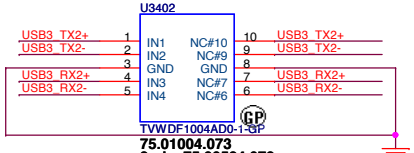


Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)

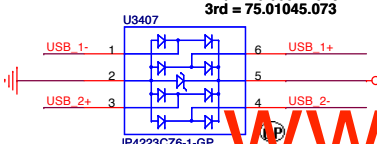


75.01004.073
2nd = 75.00524.073
3rd = 75.01045.073

Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)



75.01004.073
2nd = 75.00524.073
3rd = 75.01045.073



75.04223.07C
2nd = 75.12304.07C

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 2.0/ 3.0 Port**

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 34 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

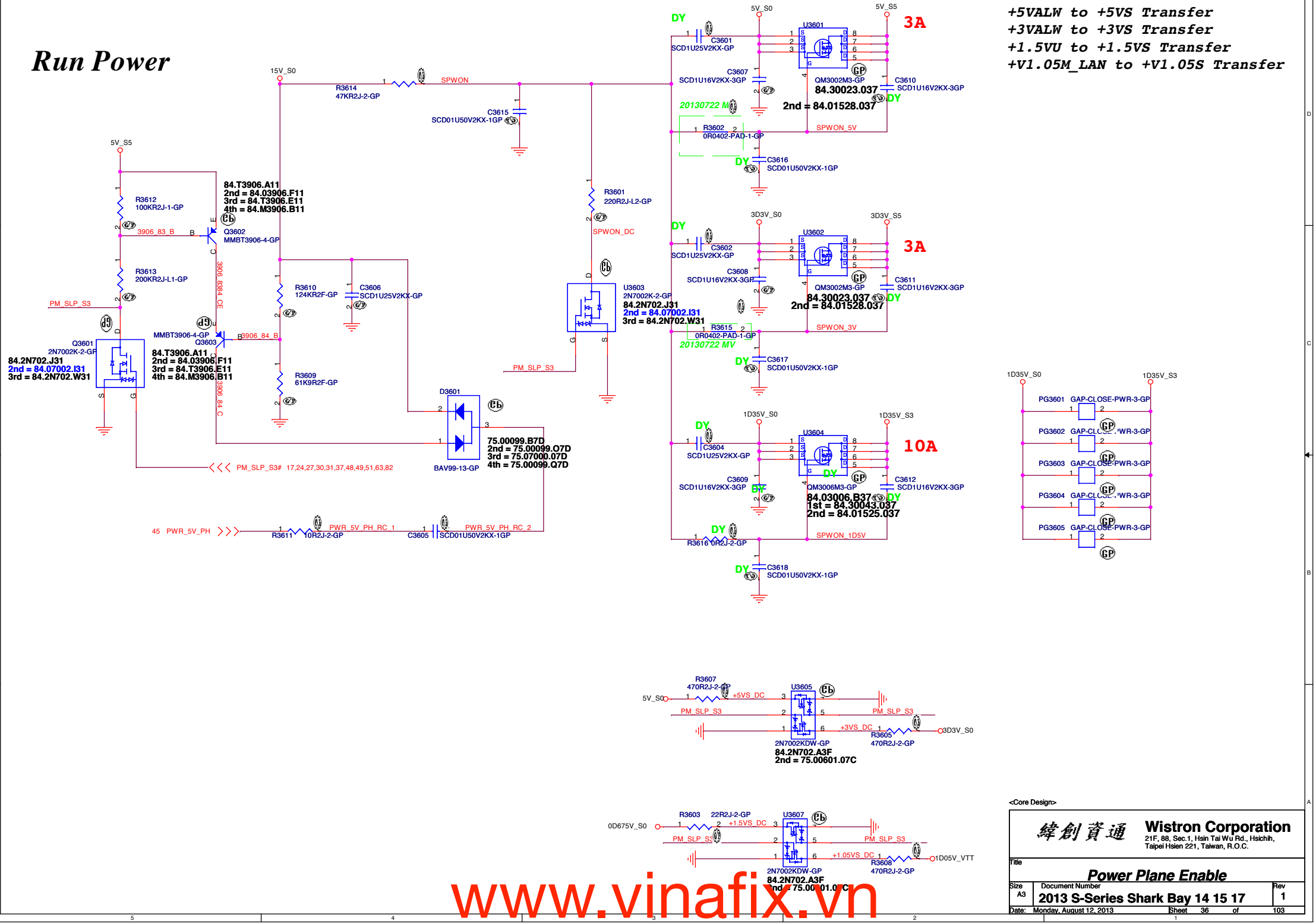
Title
USB Charger

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 35 of 103

Run Power

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

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A3	2013 S-Series Shark Bay 14 15 17	1

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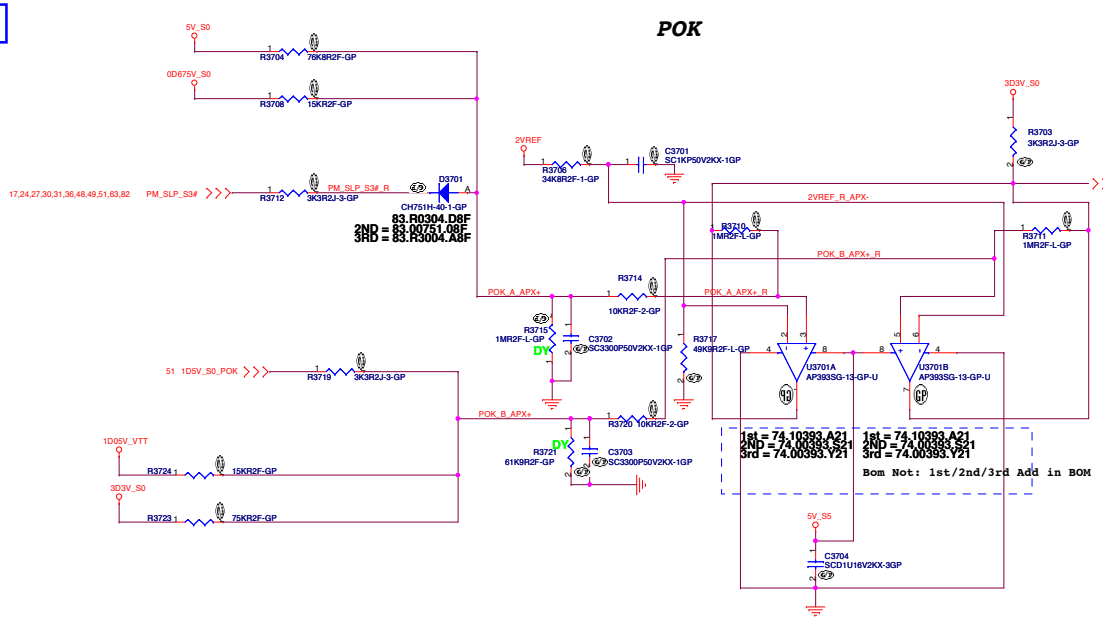
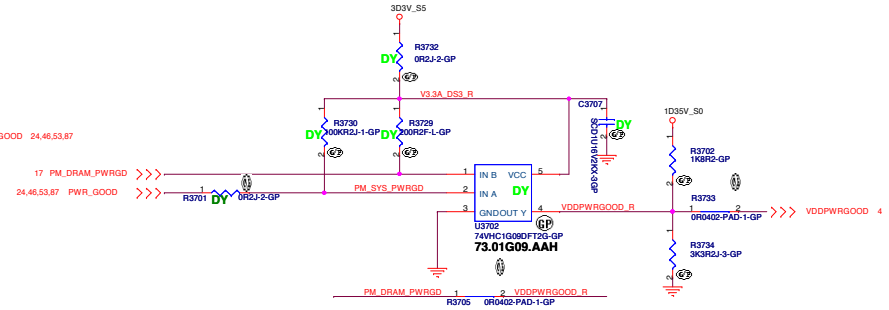
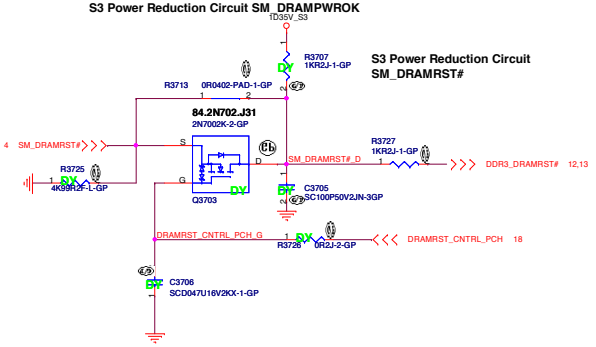
POK



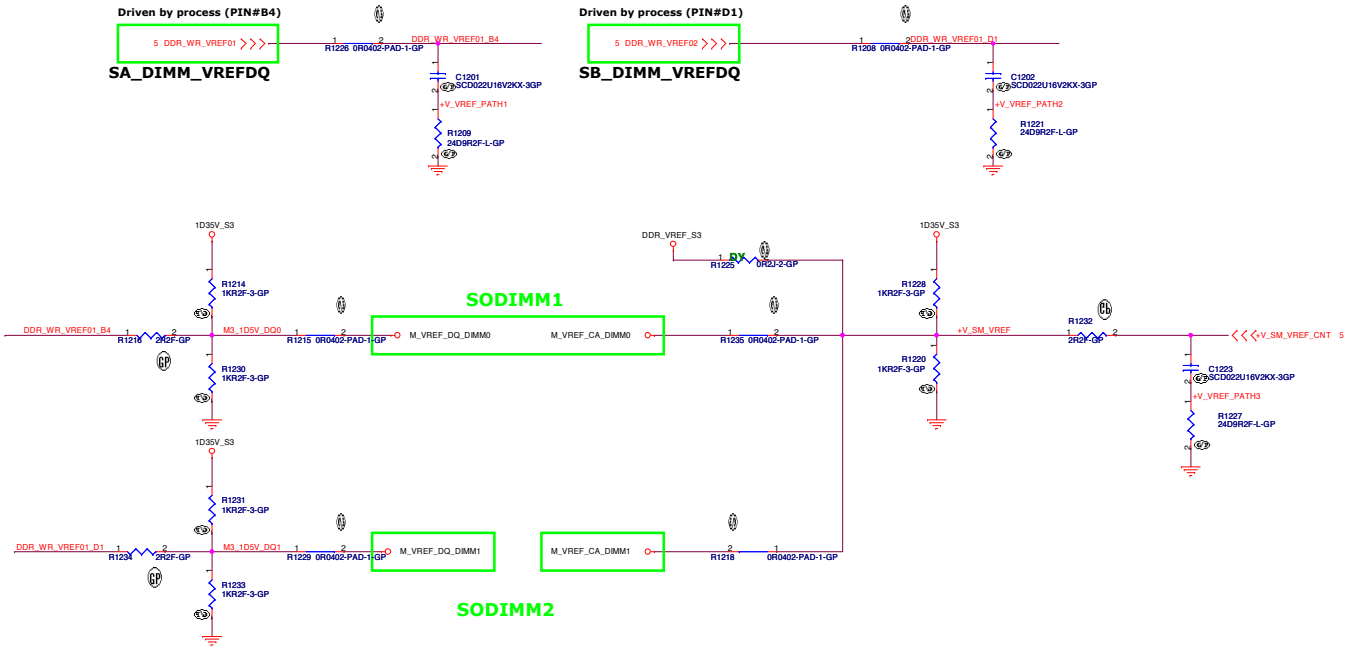
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POK

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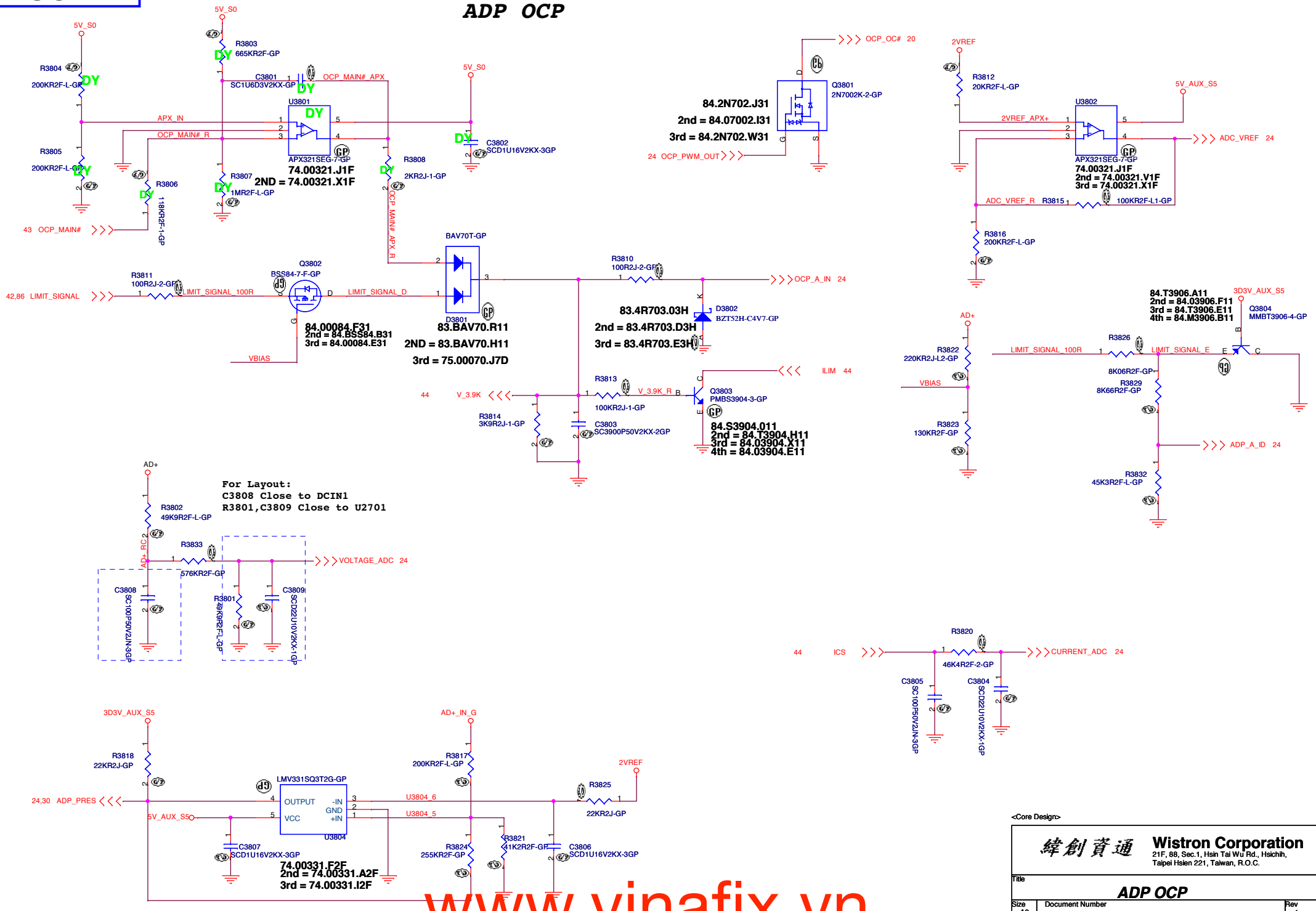
ADP OCP

ADP OCP



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP OCP

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 38 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D05_M*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 39 of 103

<Variant Name>

Title	<Title>	
Size A2	Document Number 2013 S-Series Shark Bay 14 15 17	Rev 1
Date: Wednesday, July 03, 2013	Sheet 40 of 103	

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51225_5V/3D3V

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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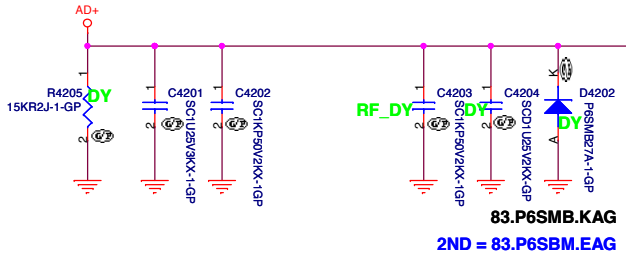
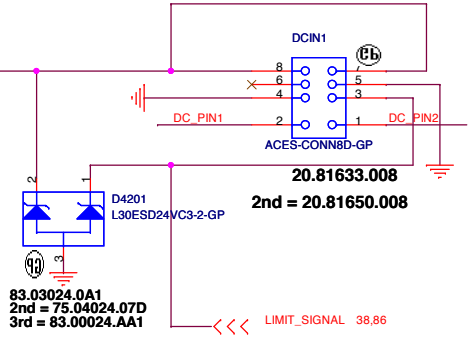
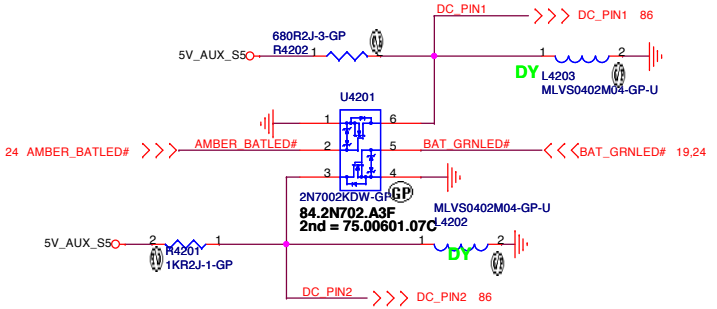
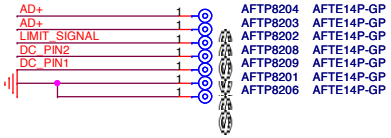
Adaptor in to generate DCBATOUT

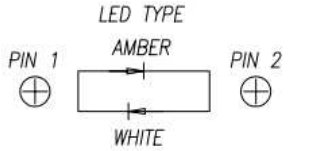








	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low



NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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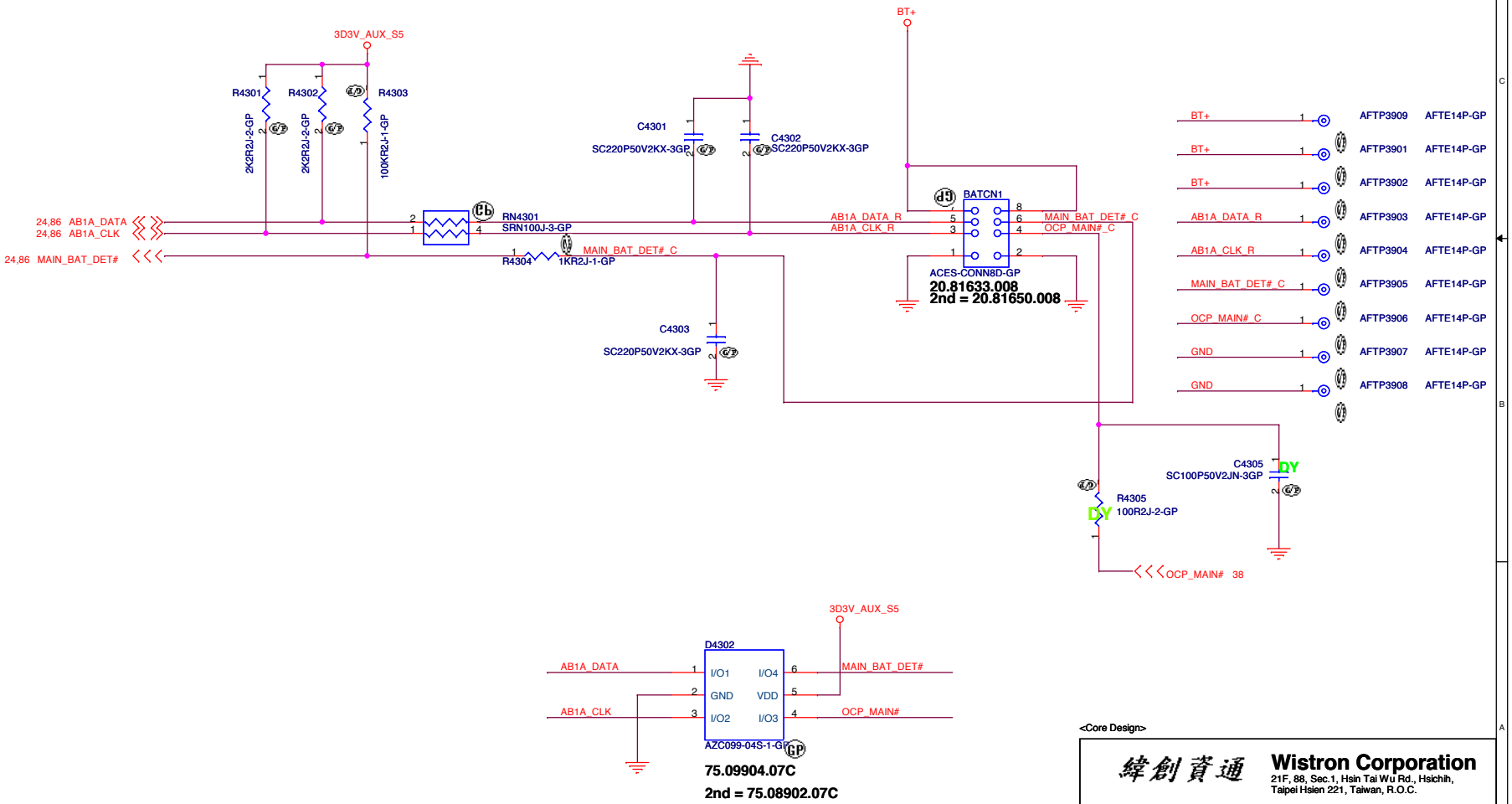
Battery Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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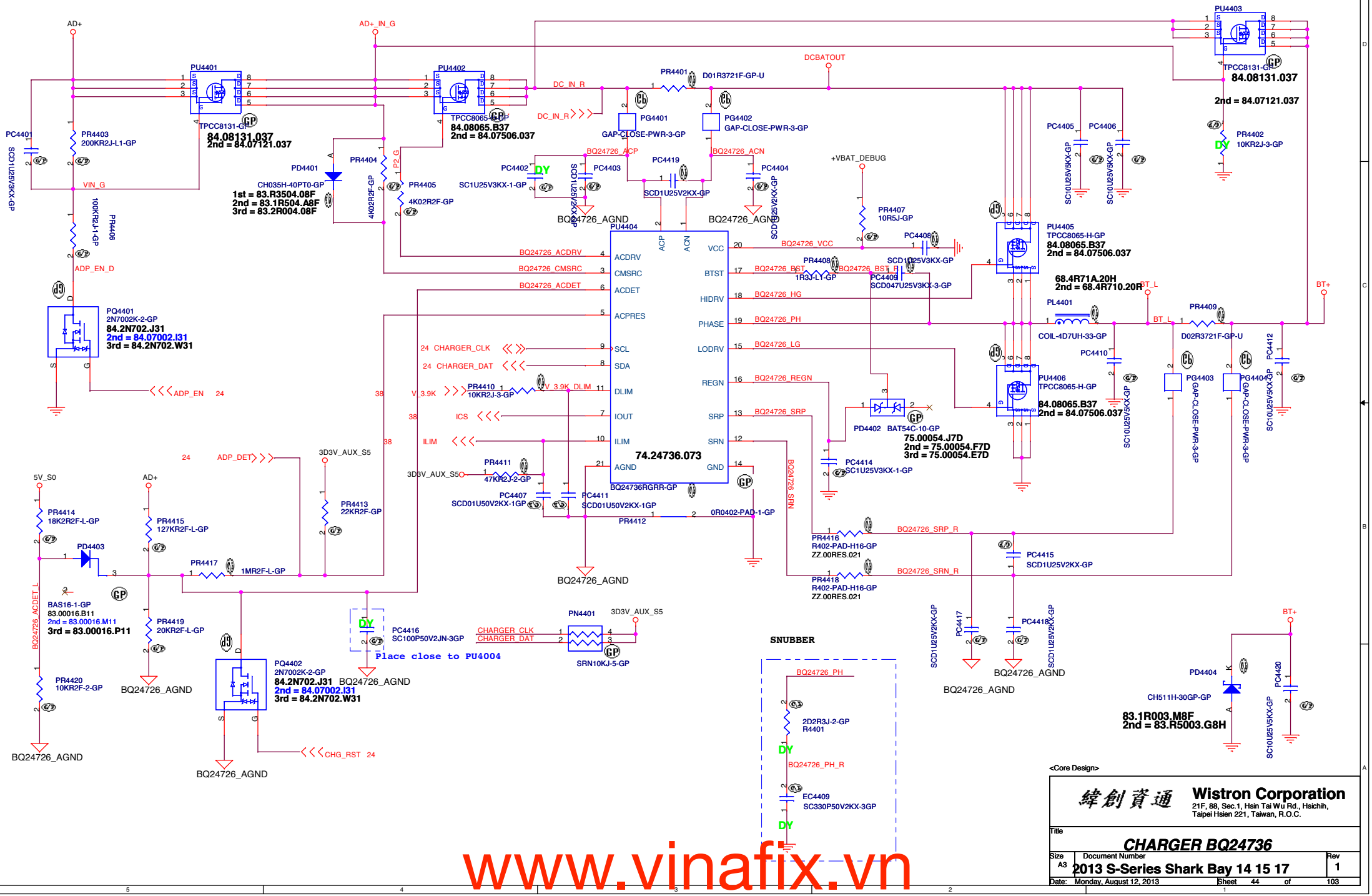
BQ24736 for CHARGER



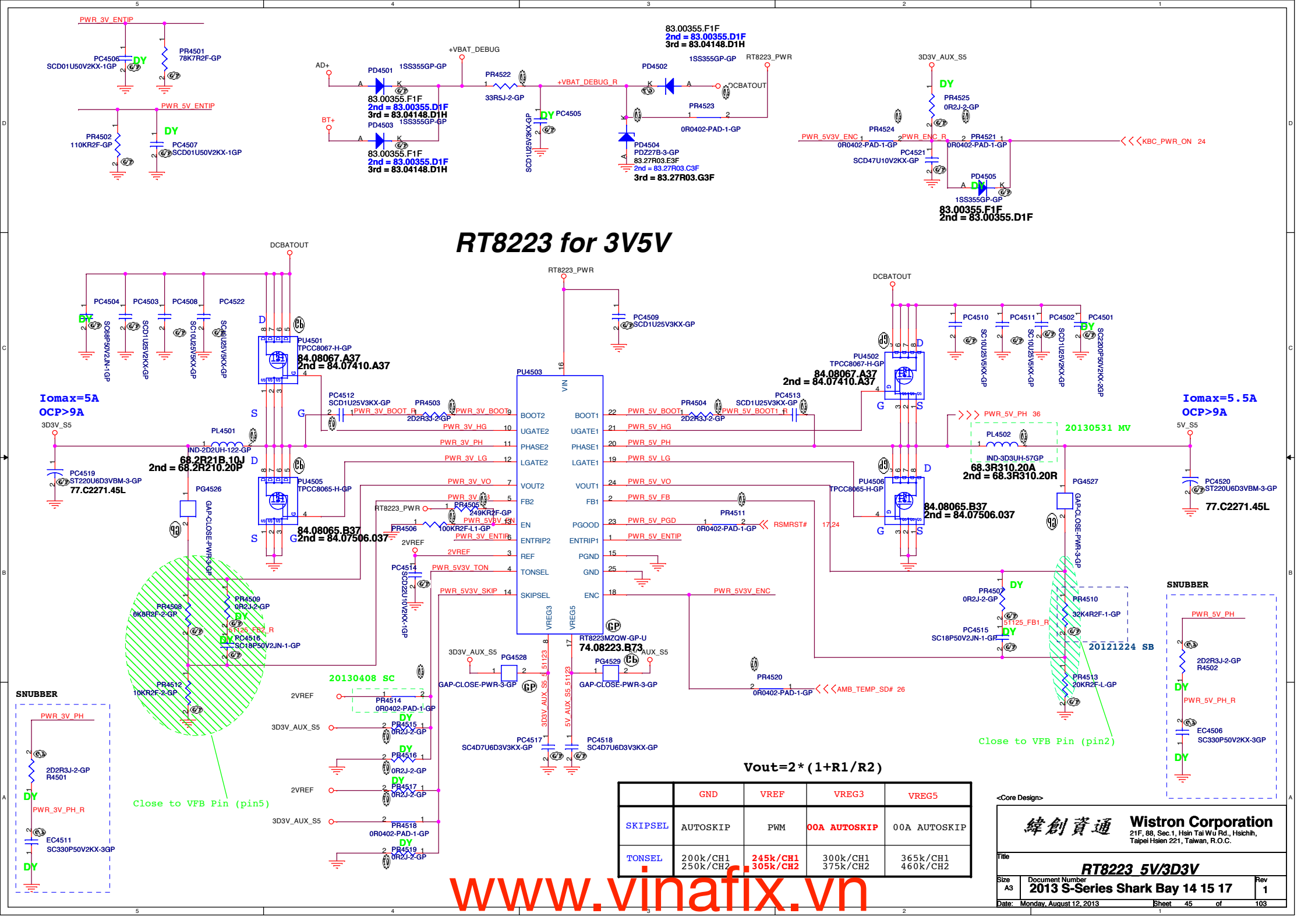
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24736

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 44 of 103


RT8223 for 3V5V
PWR_3V_ENTIP
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SCD01U50V2KX-1GP
PR4501
78K7R2F-GP
PWR_5V_ENTIP
PR4502
110KR2F-GP
PC4507
SCD01U50V2KX-1GP
+VBAT_DEBUG
AD+
BT+
PD4501
PD4503
1SS355GP-GP
PR4522
33R5J-2-GP
+VBAT_DEBUG_R
PC4505
SCD1U25V3KX-GP
PD4502
PD4504
PDZ27B-3-GP
RT8223_PWR
DCBATOUT
PR4523
0R0402-PAD-1-GP
83.00355.F1F
2nd = 83.00355.D1F
3rd = 83.04148.D1H
83.27R03.E3F
2nd = 83.27R03.C3F
3rd = 83.27R03.G3F
3D3V_AUX_S5
PR4525
0R2J-2-GP
PR4524
PWR_5V3V_ENC
PWR_ENC_R
PR4521
KBC_PWR_ON 24
PC4521
SCD47U10V2KX-GP
PD4505
DCBATOUT
PC4504
PC4503
PC4508
PC4522
SC68P50V2JN-1GP
SCD1U25V2KX-GP
SC10U25V5KX-GP
PU4501
TPCC8067-H-GP
84.08067.A37
2nd = 84.07410.A37
PC4512
SCD1U25V3KX-GP
PR4503
2D2R3J-2-GP
PWR_3V_BOOT_R
PWR_3V_BOOT
PWR_3V_HG
PWR_3V_PH
PWR_3V_LG
PWR_3V_VO
PWR_3V_FB
PWR_5V3V_TON
PWR_5V3V_SKIP
PWR_3V_ENTIP
2VREF
PR4505
249KR2F-GP
PR4506
100KR2F-L1-GP
PU4503
VIN
BOOT2
UGATE2
PHASE2
LGATE2
VOUT2
FB2
EN
ENTRIP2
REF
TONSEL
SKIPSEL
BOOT1
UGATE1
PHASE1
LGATE1
VOUT1
FB1
PGOOD
ENTRIP1
PGND
GND
ENC
VREG3
VREG5
RT8223MZQW-GP-U
74.08223.B73
PC4509
SCD1U25V3KX-GP
PC4513
SCD1U25V3KX-GP
PR4504
2D2R3J-2-GP
PWR_5V_BOOT
PWR_5V_BOOT1_R
PWR_5V_HG
PWR_5V_PH
PWR_5V_LG
PWR_5V_VO
PWR_5V_FB
PWR_5V_PGD
PWR_5V_ENTIP
PWR_5V3V_ENC
PR4511
0R0402-PAD-1-GP
RSMRST#
17,24
PR4520
AMB_TEMP_SD# 26
PC4514
SCD22U10V2KX-1GP
PR4508
6K8R2F-2-GP
PR4509
0R2J-2-GP
PC4516
SC18P50V2JN-1-GP
PR4512
10KR2F-2-GP
PG4526
GAP-CLOSE-PWR-3-GP
PG4528
PG4529
3D3V_AUX_S5
5V_AUX_S5
PC4517
SC4D7U6D3V3KX-GP
PC4518
SC4D7U6D3V3KX-GP
PU4502
TPCC8067-H-GP
84.08067.A37
2nd = 84.07410.A37
PU4506
TPCC8065-H-GP
84.08065.B37
2nd = 84.07506.037
PC4510
PC4511
PC4502
PC4501
SC220P50V2KX-2GP
PWR_5V_PH 36
PL4502
IND-3D3UH-57GP
68.3R310.20A
2nd = 68.3R310.20R
20130531 MV
PG4527
PR4507
0R2J-2-GP
PC4515
SC18P50V2JN-1-GP
PR4510
32K4R2F-1-GP
PR4513
20KR2F-L-GP
20121224 SB
PC4520
ST220U6D3VBM-3-GP
77.C2271.45L
Iomax=5A
OCP>9A
Iomax=5.5A
OCP>9A
3D3V_S5
5V_S5
PL4501
IND-2D2UH-122-GP
68.2R21B.10J
2nd = 68.2R210.20P
PC4519
ST220U6D3VBM-3-GP
77.C2271.45L
20130408 SC
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
SNUBBER
PWR_3V_PH
2D2R3J-2-GP
R4501
PWR_3V_PH_R
EC4511
SC330P50V2KX-3GP
PWR_5V_PH
2D2R3J-2-GP
R4502
PWR_5V_PH_R
EC4506
SC330P50V2KX-3GP
Vout=2*(1+R1/R2)
GND
VREF
VREG3
VREG5
SKIPSEL
AUTOSKIP
PWM
00A AUTOSKIP
00A AUTOSKIP
TONSEL
200k/CH1
250k/CH2
245k/CH1
305k/CH2
300k/CH1
375k/CH2
365k/CH1
460k/CH2
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8223_5V/3D3V
Size
A3
Document Number
2013 S-Series Shark Bay 14 15 17
Rev
1
Date: Monday, August 12, 2013
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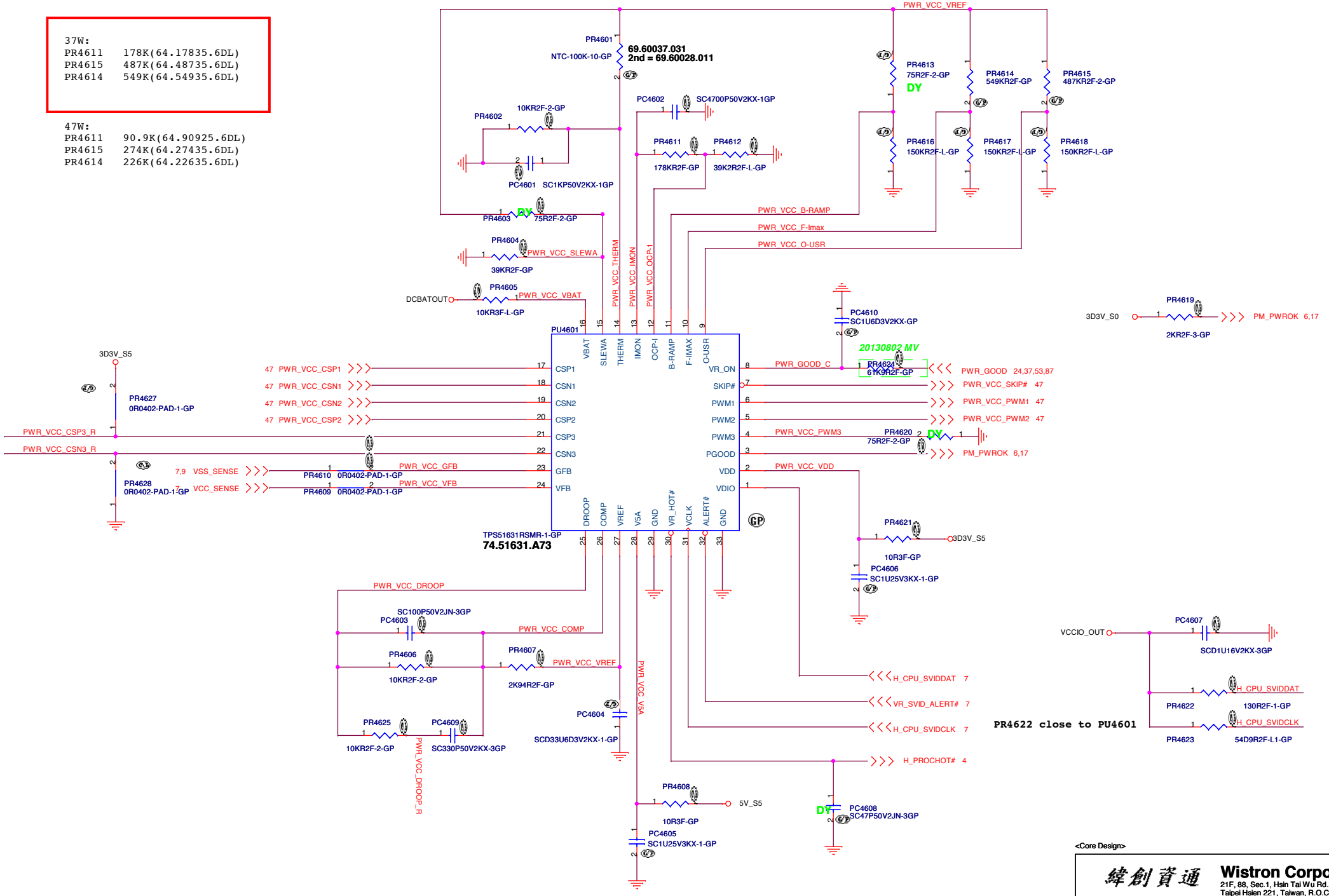
www.vinafix.vn

37W:
PR4611 178K(64.17835.6DL)
PR4615 487K(64.48735.6DL)
PR4614 549K(64.54935.6DL)

47W:
PR4611 90.9K(64.90925.6DL)
PR4615 274K(64.27435.6DL)
PR4614 226K(64.22635.6DL)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51631_CPUCORE(1/2)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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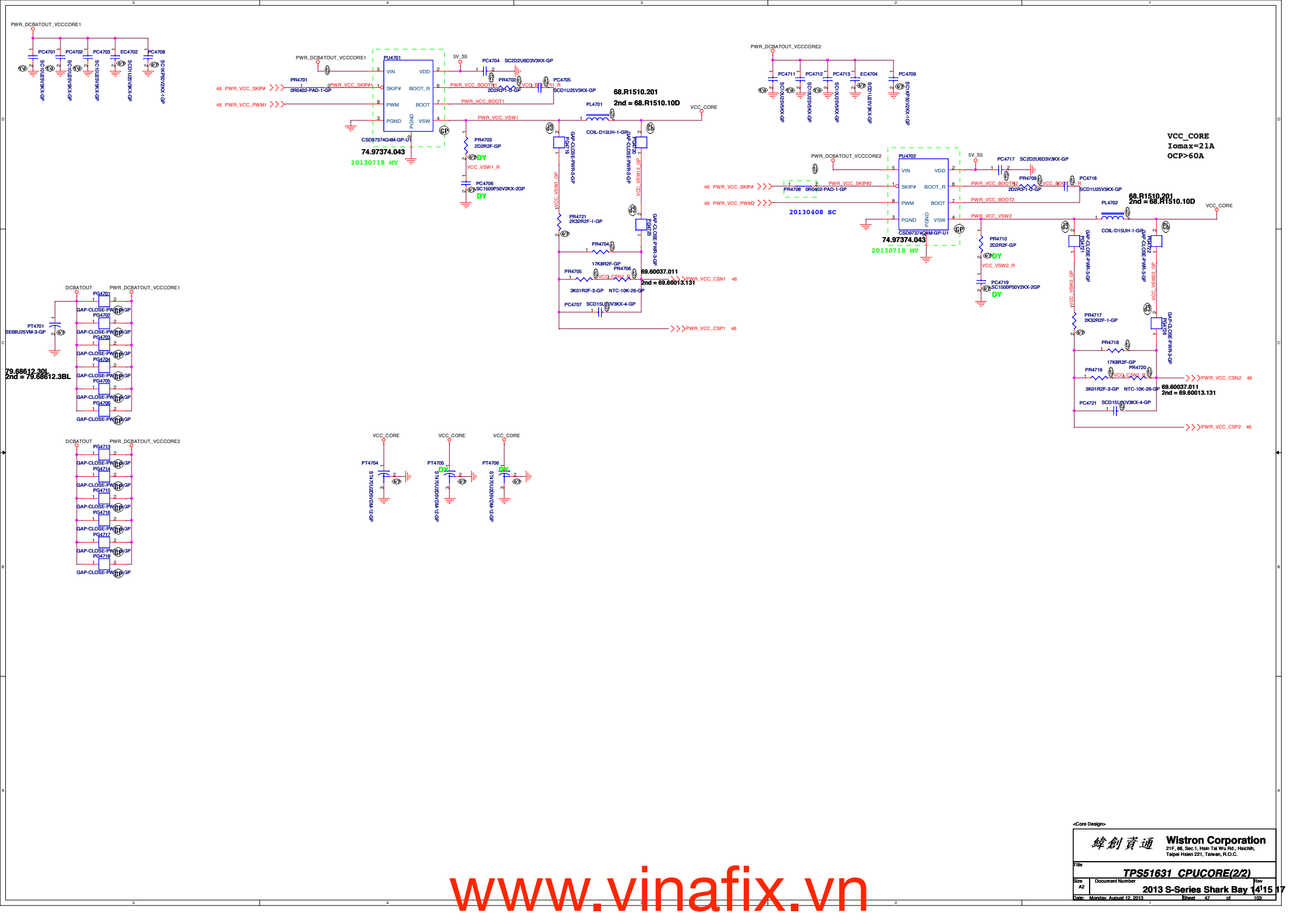


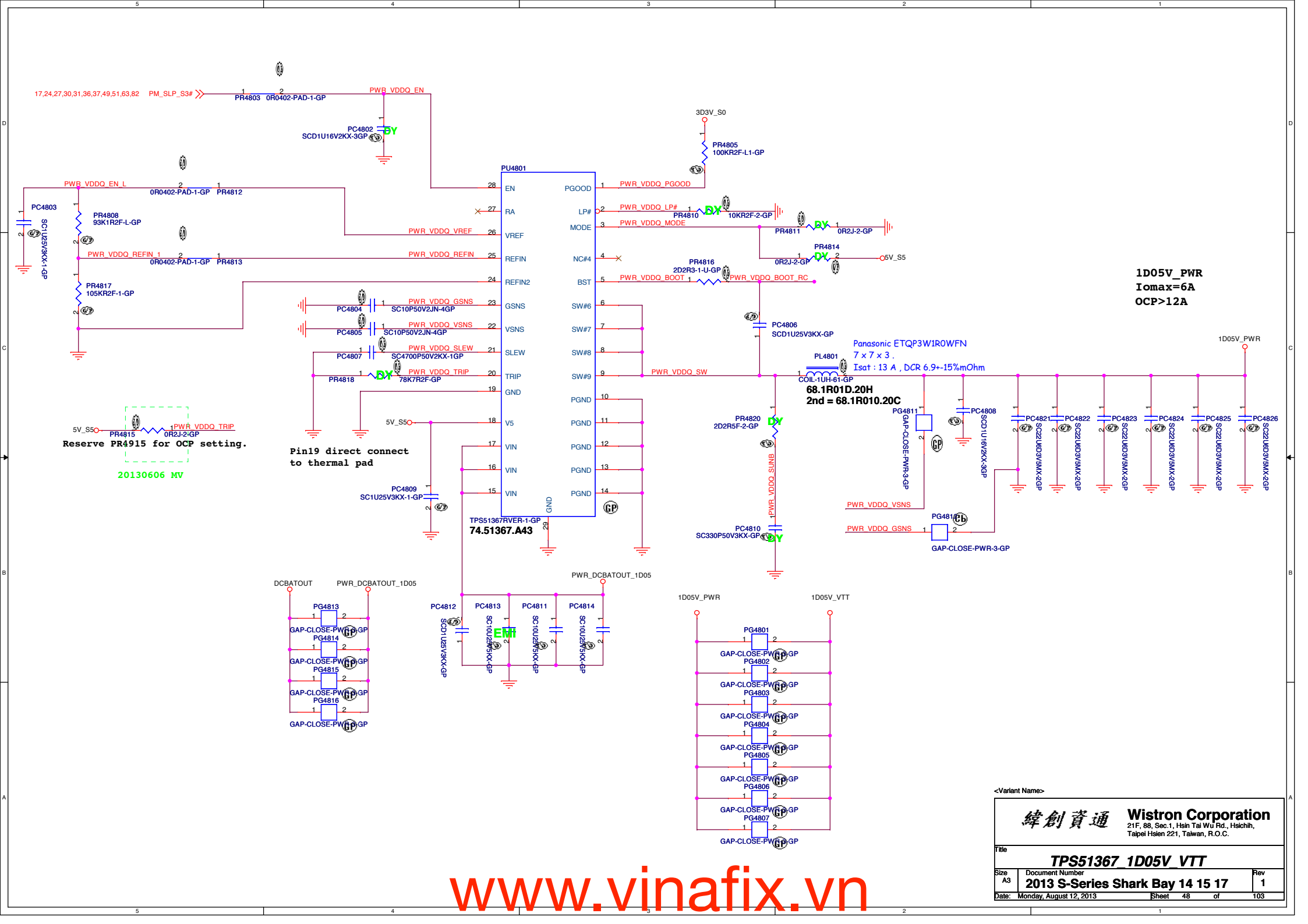
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51631 CPUCORE(2/2)

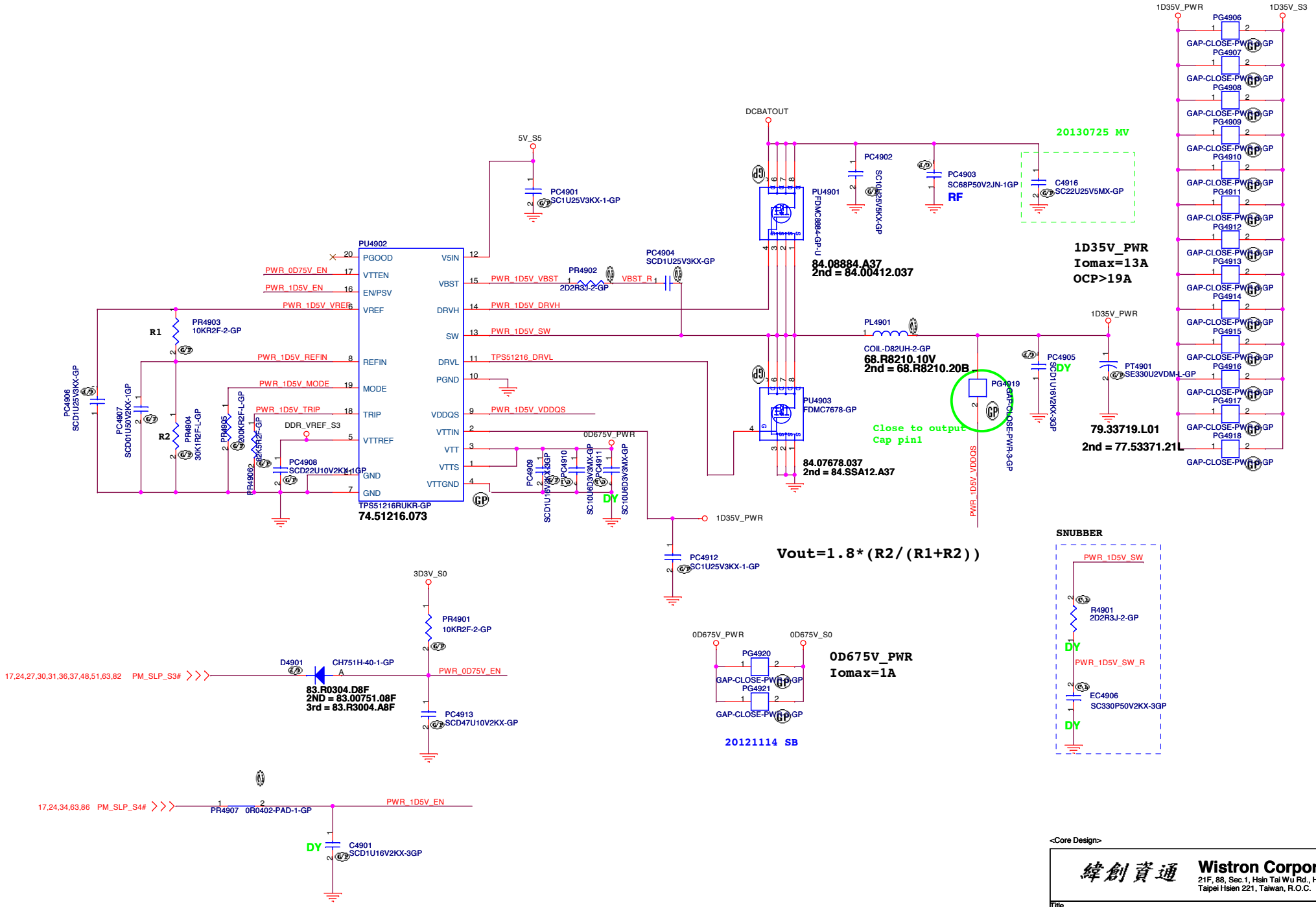
Size: A2 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev:

Date: Monday, August 12, 2013 | Sheet 47 of 103



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***TPS51367_1D05V_VTT***
Size: A3	Document Number: **2013 S-Series Shark Bay 14 15 17**
Rev: 1	
Date: Monday, August 12, 2013	Sheet 48 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_1D35V & 0D675V

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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(Blanking)

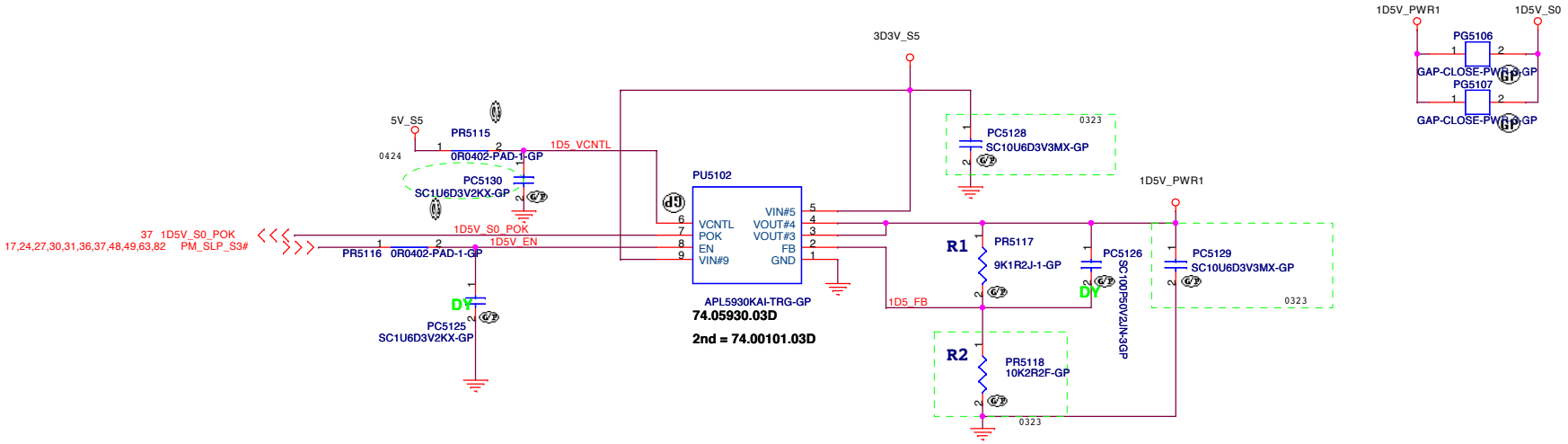
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev:

Date: Wednesday, July 03, 2013 | Sheet 50 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930_1D5V_S0

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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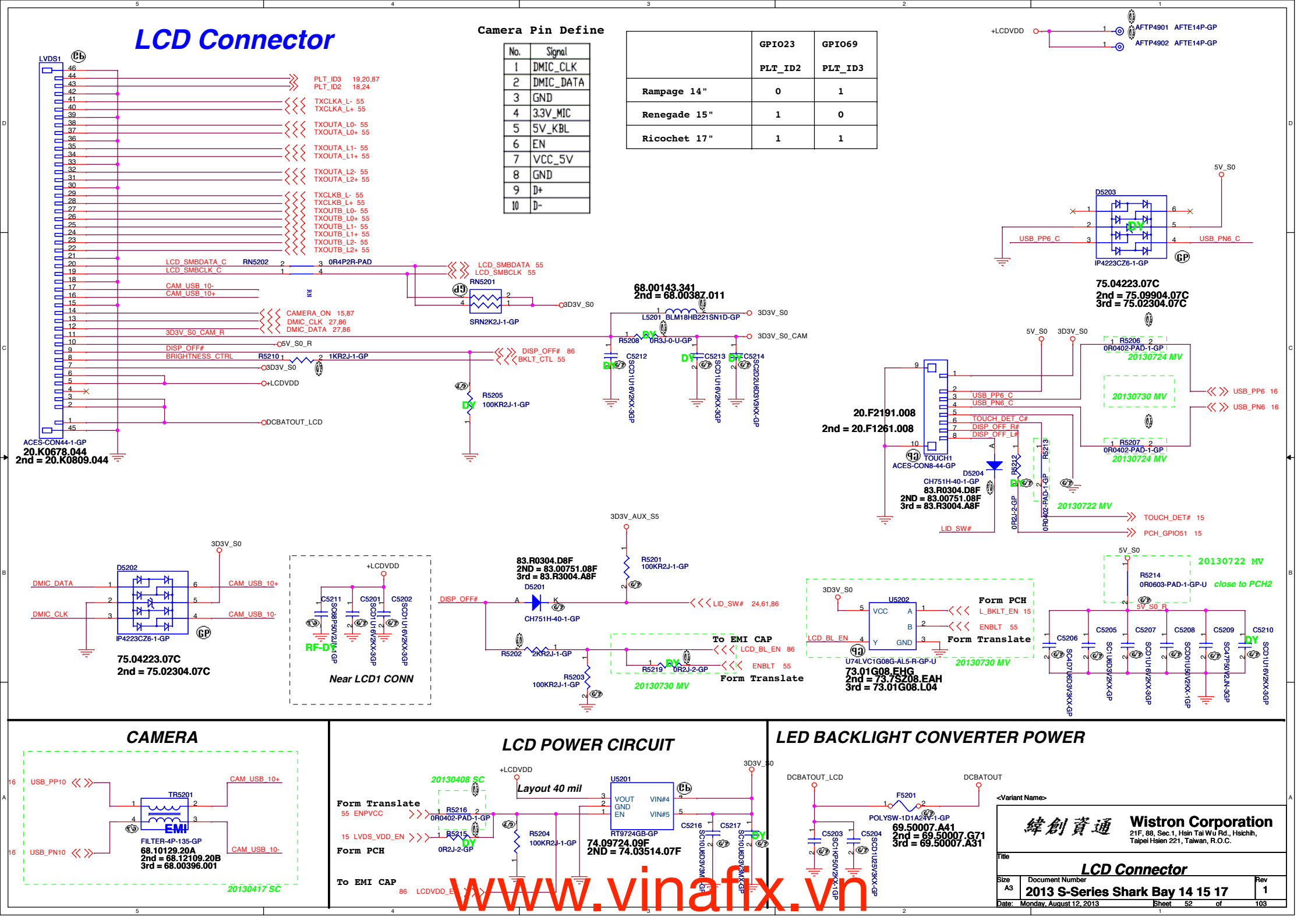
LCD Connector

Camera Pin Define

No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-

	GPIO23 PLT_ID2	GPIO69 PLT_ID3
Rampage 14"	0	1
Renegade 15"	1	0
Ricochet 17"	1	1



CAMERA

LCD POWER CIRCUIT

LED BACKLIGHT CONVERTER POWER

<Variant Name>

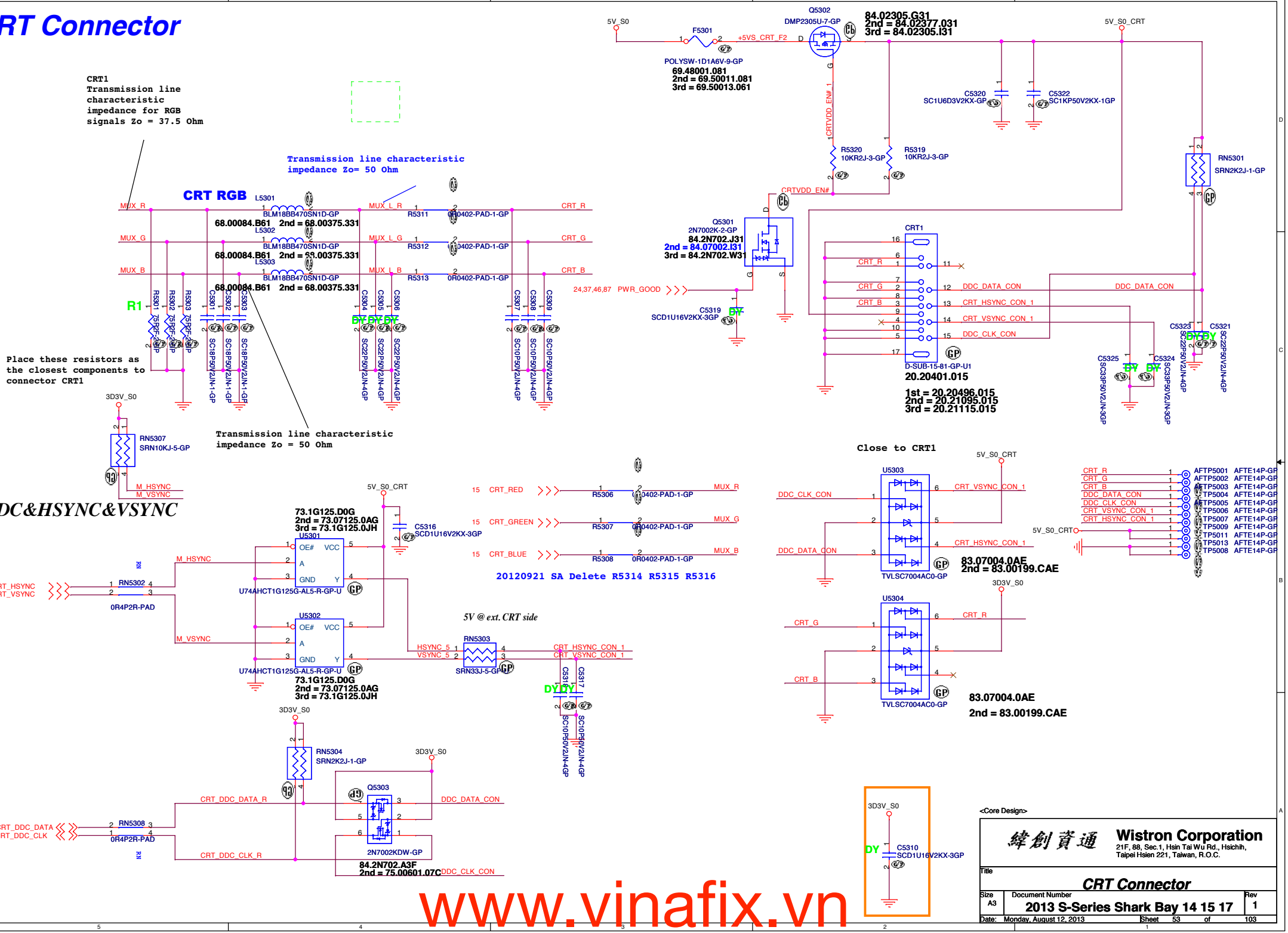
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

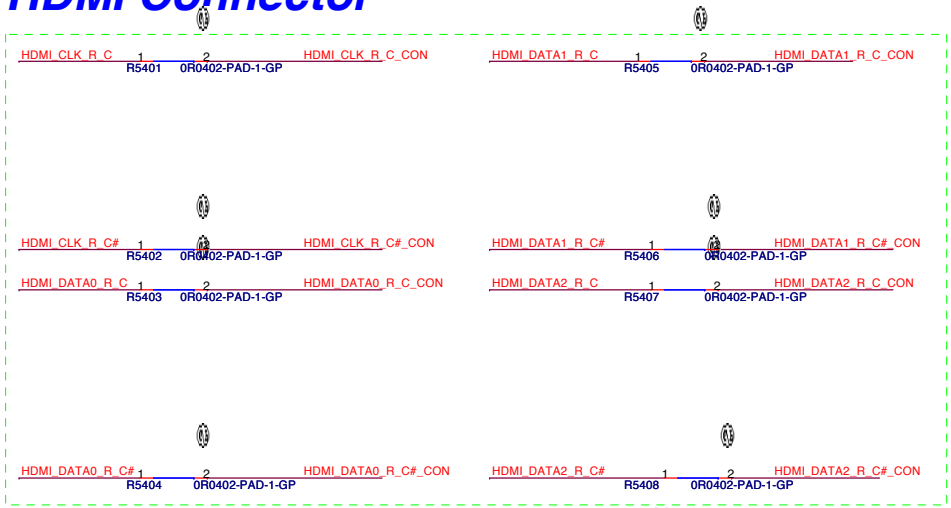
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 52 of 103

CRT Connector

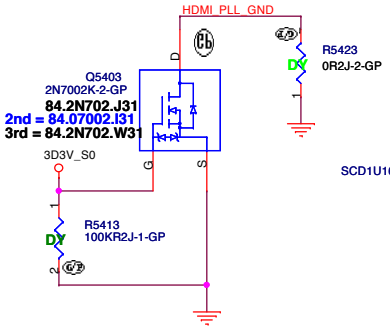


HDMI Connector

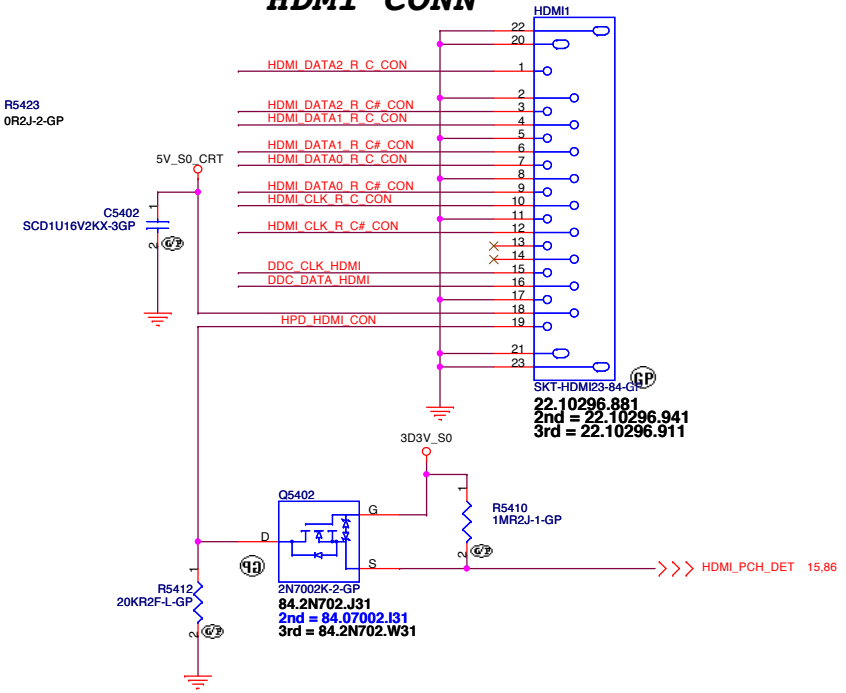


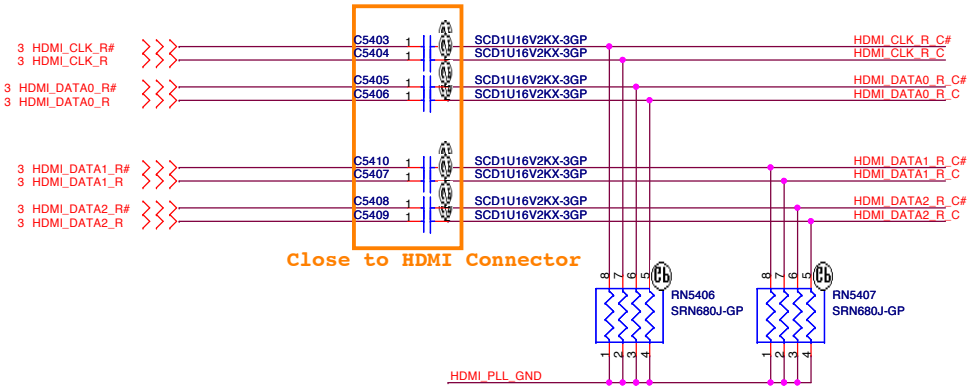
20130710 MV

20120924 SA Add R5401 ~ R5408



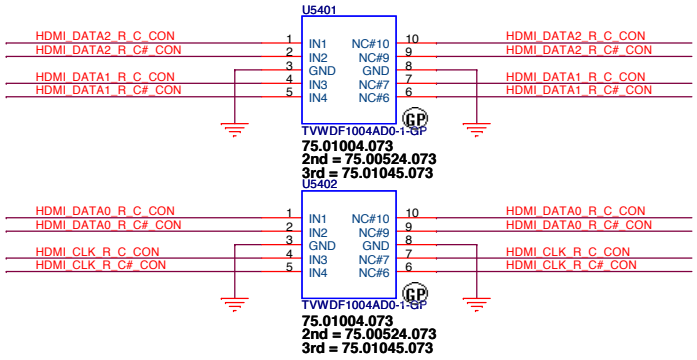
HDMI CONN

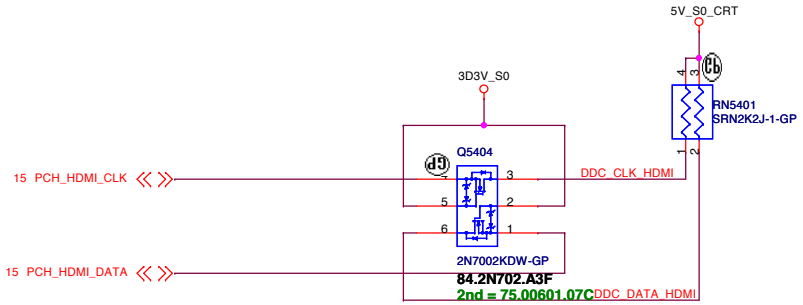




Close to HDMI Connector

Close to HDMI1





Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).

The total delay on CTRLDATA should be longer than CTRLCLK.

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Conn

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A3	2013 S-Series Shark Bay 14 15 17	1

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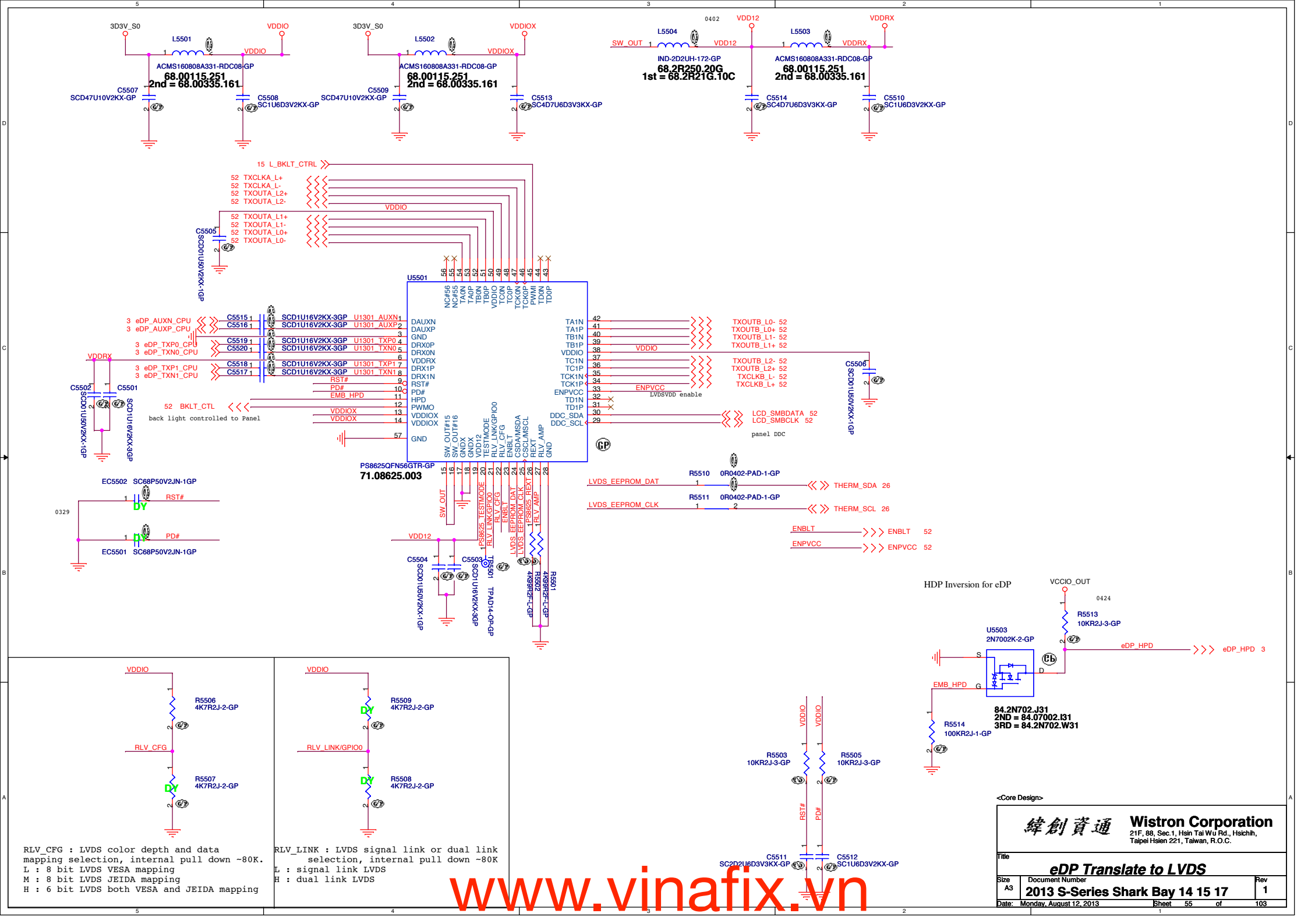
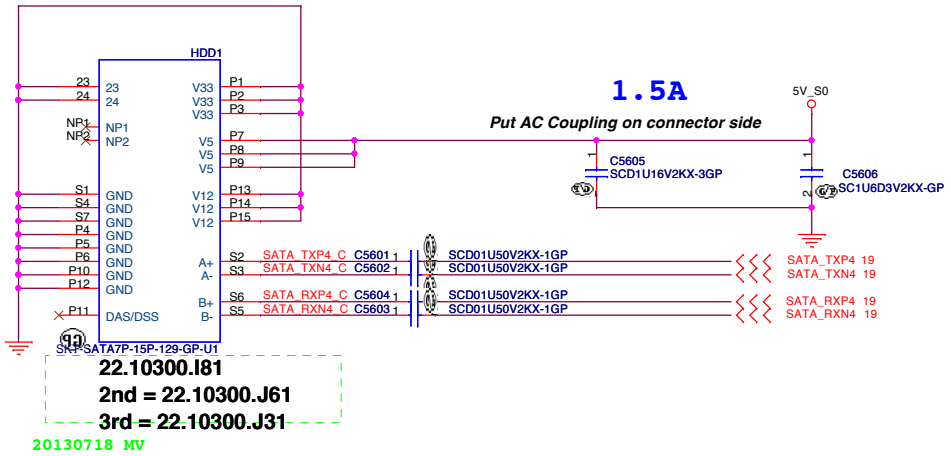
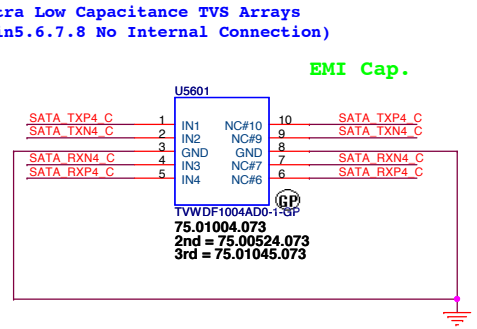
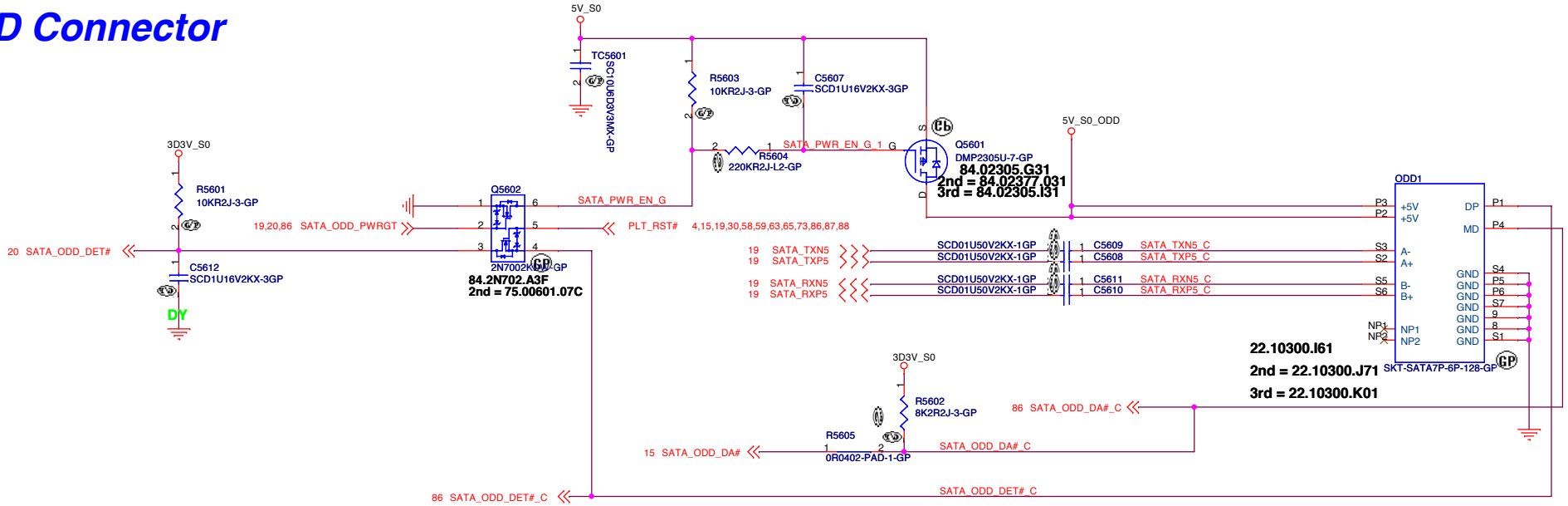


HDD Connector





ODD Connector



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
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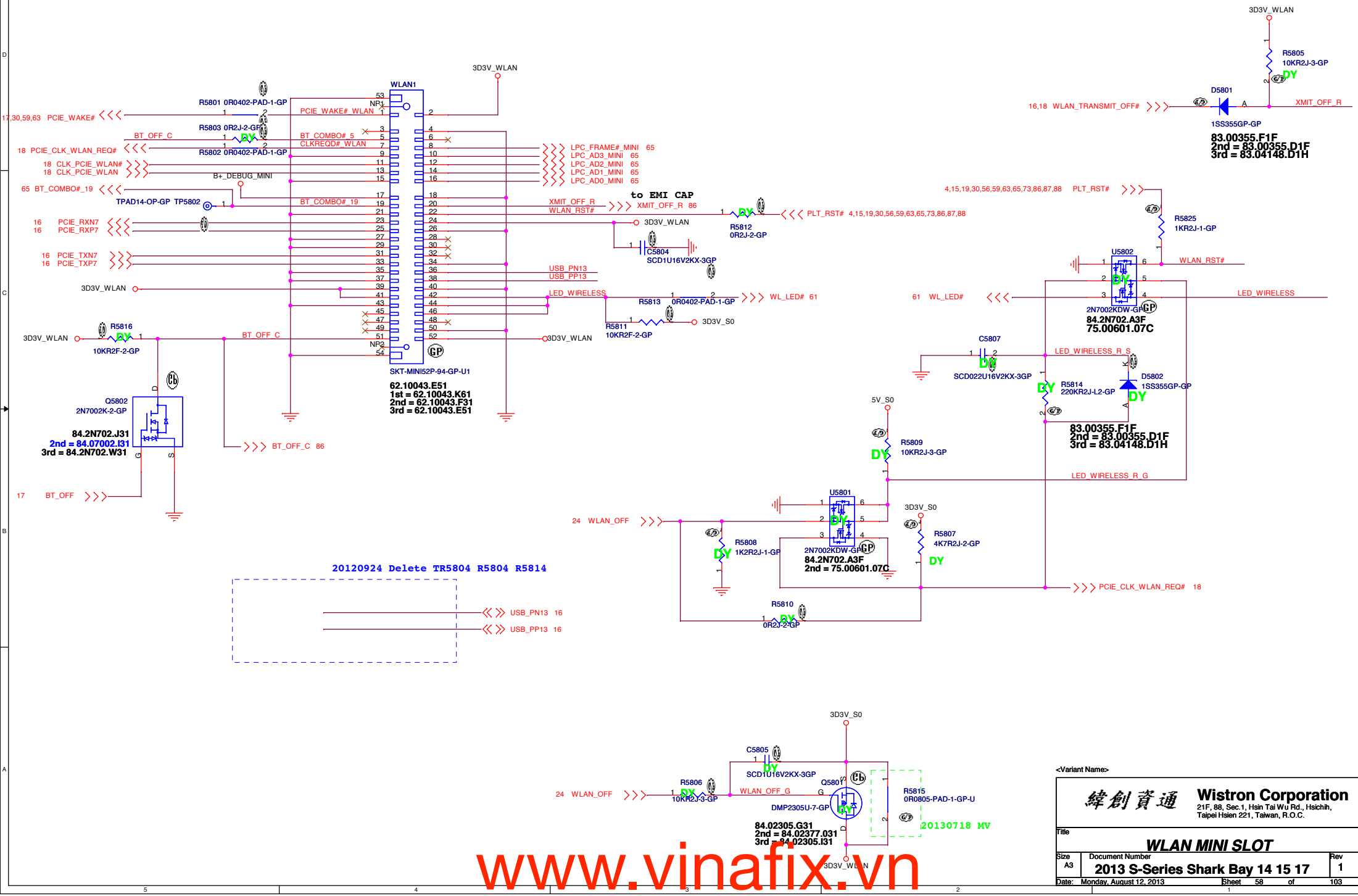
WLAN Connector

Mini-Card--WLAN (Half)



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN MINI SLOT

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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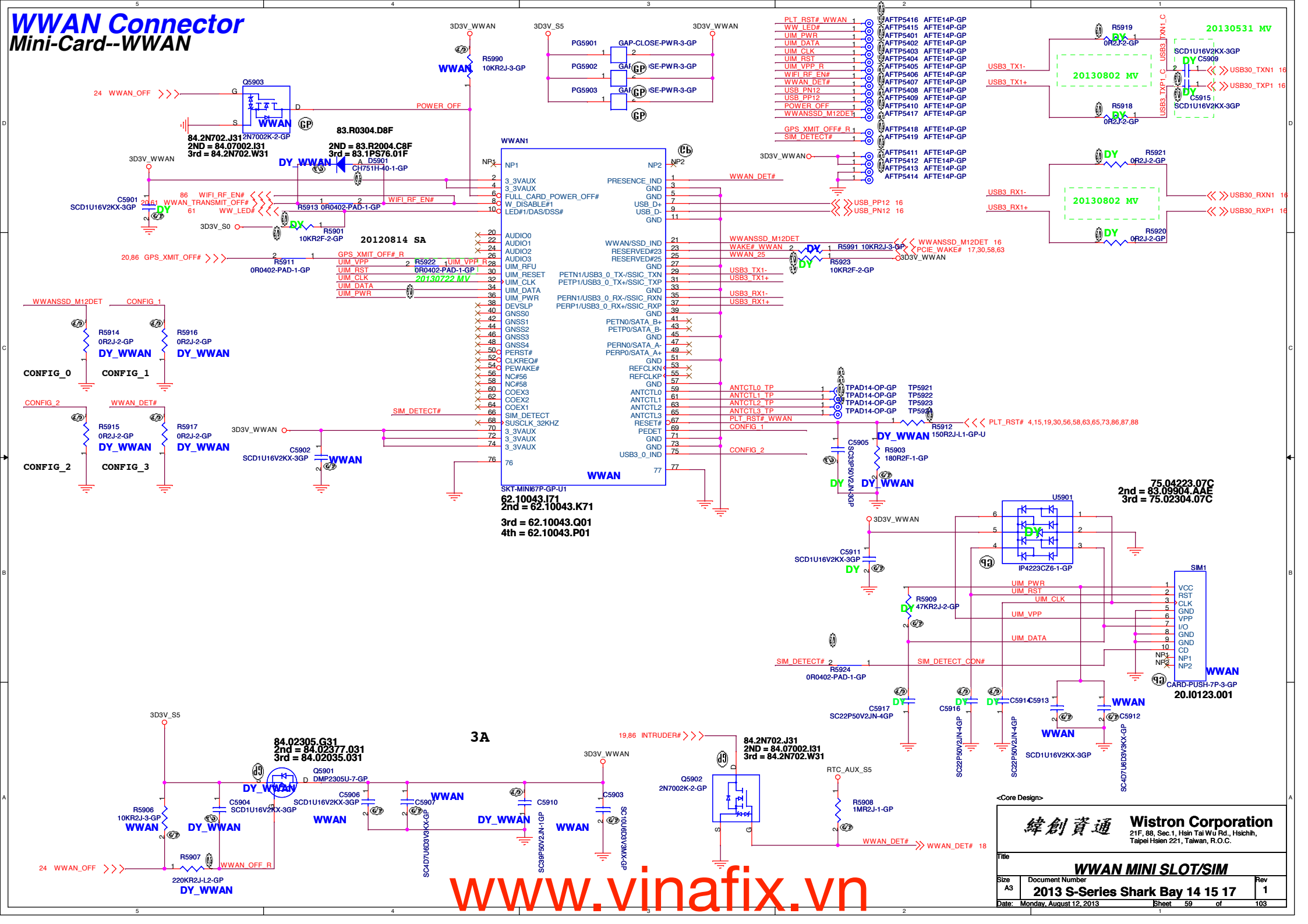
WWAN Connector
Mini-Card--WWAN



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Flash

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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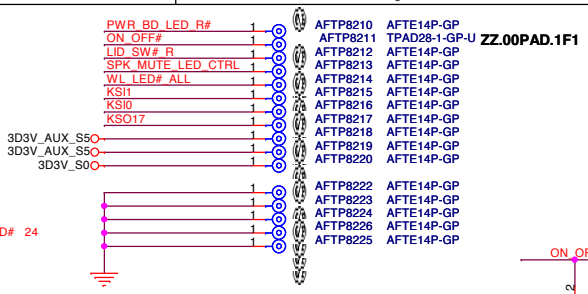
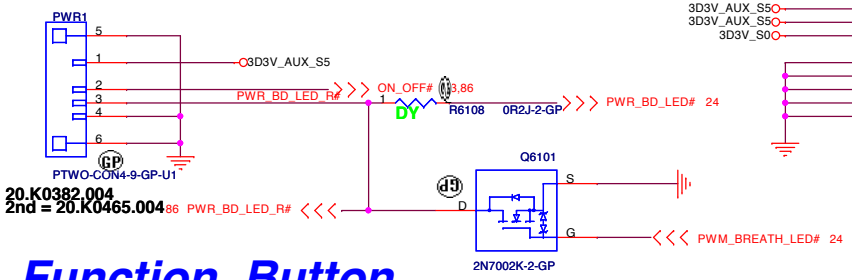
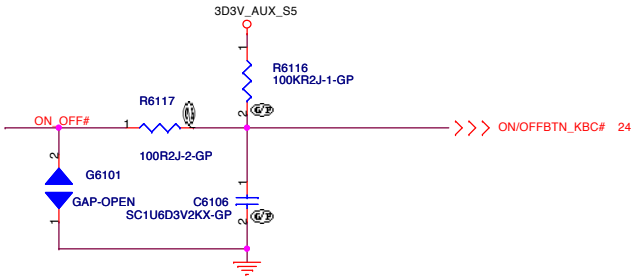
Power Button

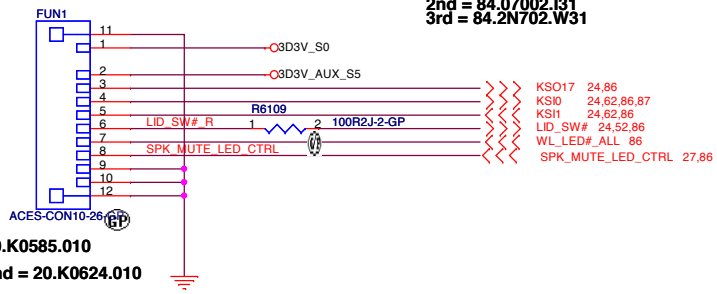


ZZ.00PAD.1F1

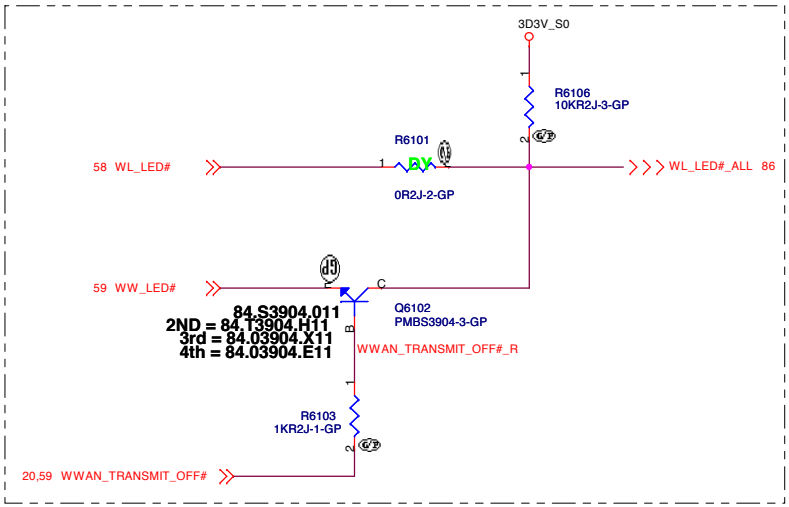


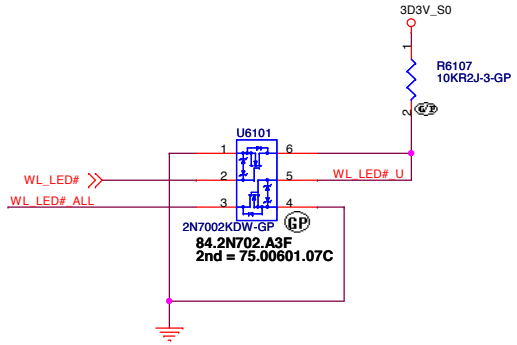


Function Button



WLAN / WWAN POWER LED





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

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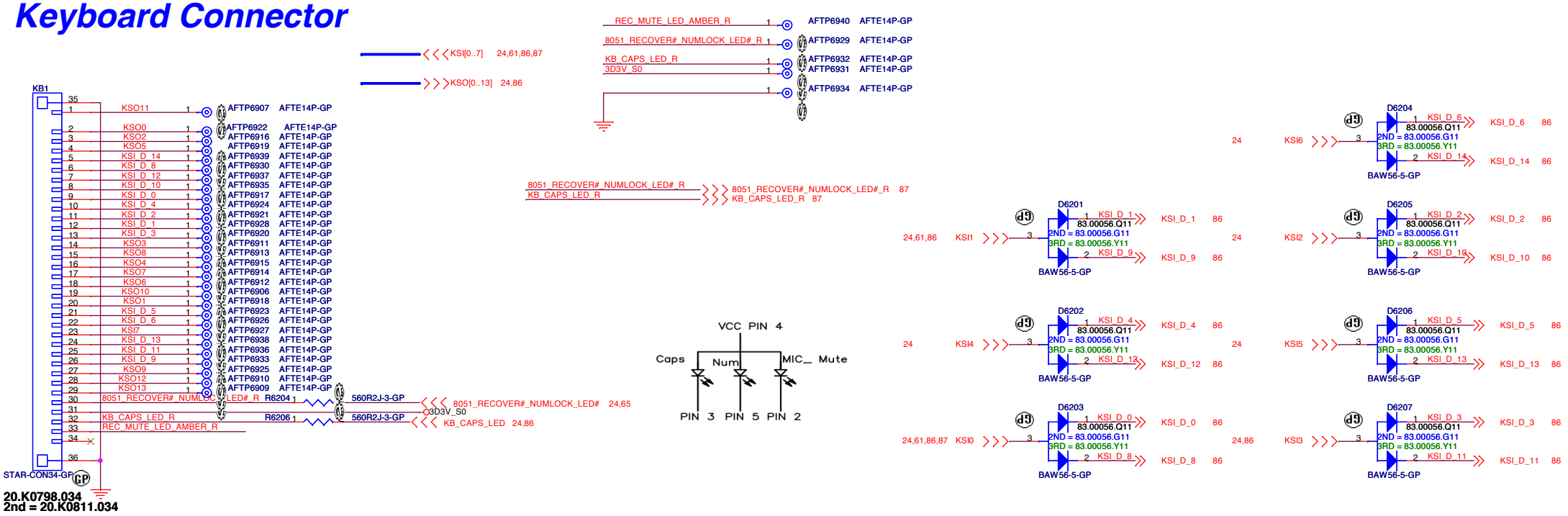
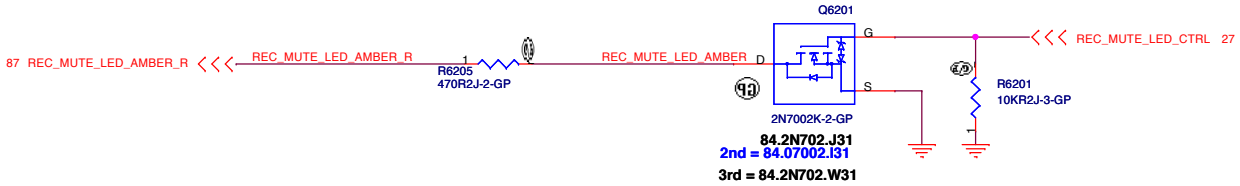
Keyboard Connector



On Keyboard LEDs

<MUTE> Internal MIC ON= No light; OFF/Mute= Amber



<Core Design>

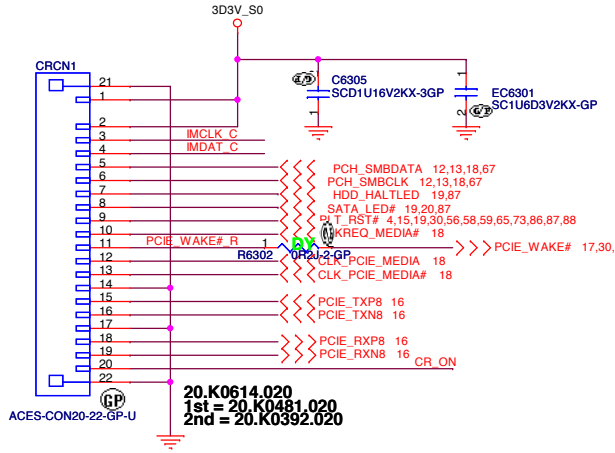
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

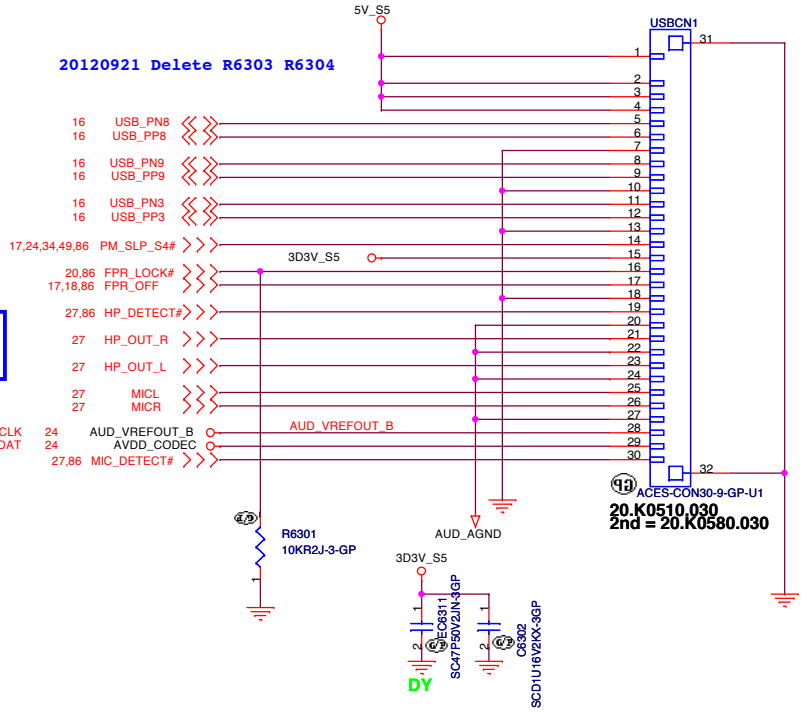
Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

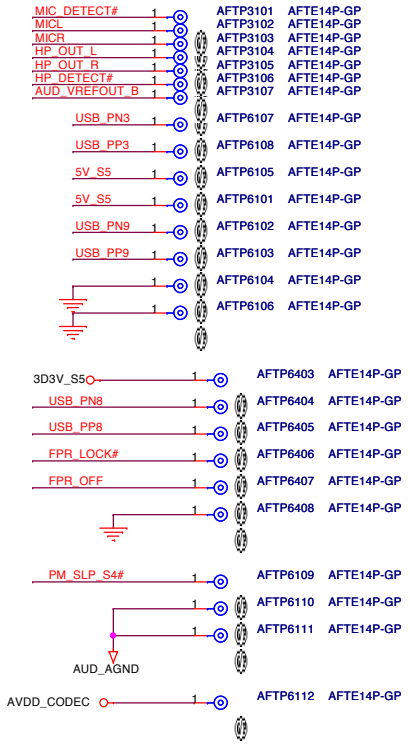
Date: Monday, August 12, 2013 Sheet 62 of 103

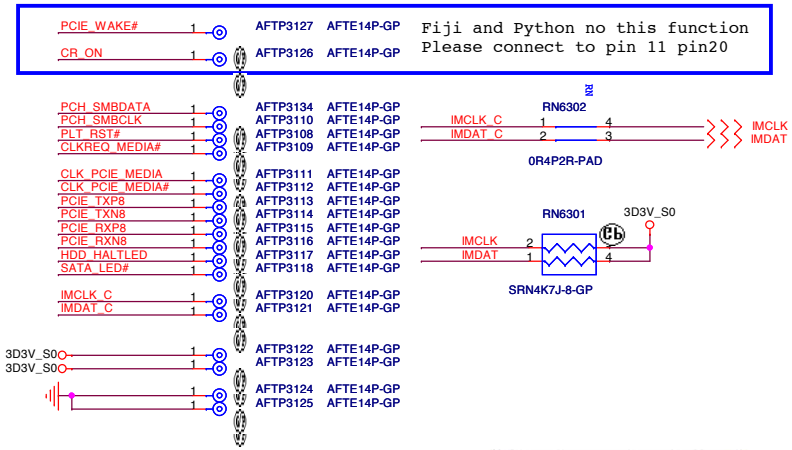
Audio Board +Touch Pad + Card Reader IC Connector



Right Side Audio & FP & USB Connector

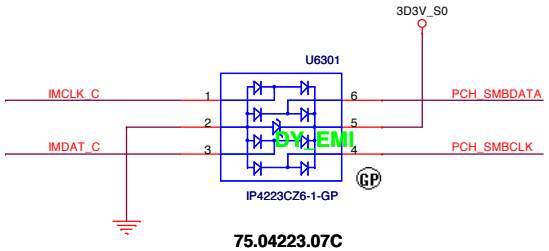






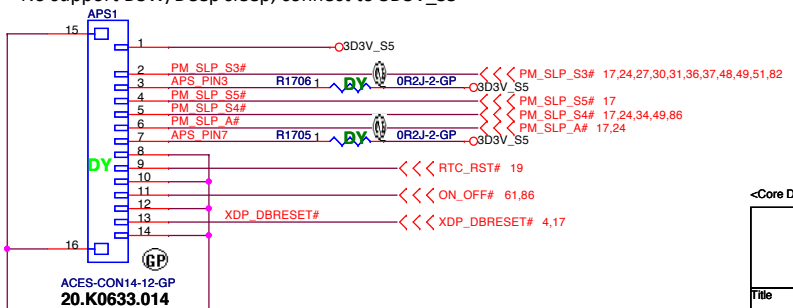
Pinout on customer's board,
as in the PDG, CDI #486713,

Pin	Signal Name
1	VccSus3_3
2	SLP_S3#
3	VccDSW3_3
4	SLP_S5#
5	SLP_S4#
6	SLP_A#
7	+V3.3DS
8	GND
9	RTCRST#
10	GND
11	PWRBTN#
12	GND
13	SYS_RESET#
14	GND



APS1 for QT test do not install

No support DSW/Deep sleep, connect to 3D3V_S5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14/15/17 | Rev:

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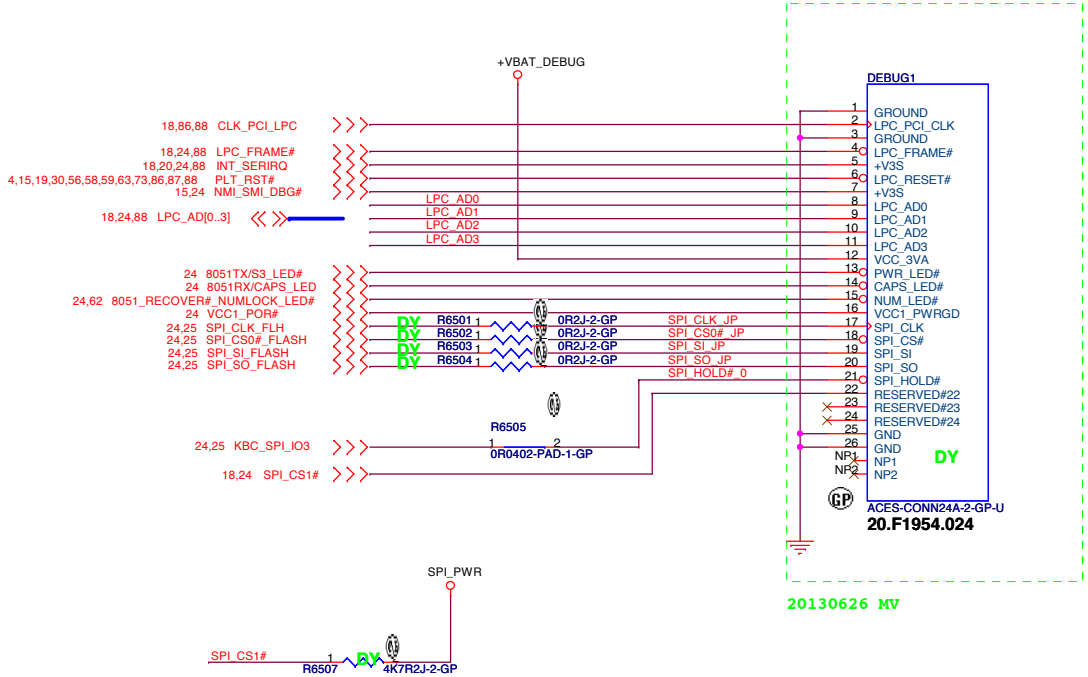
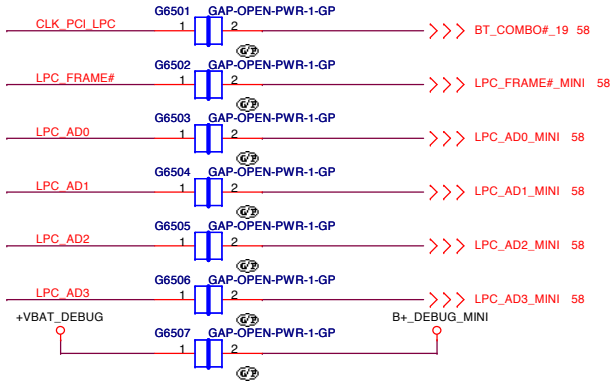
24 PIN LPC DEBUG CONN.





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

Size	Document Number	Rev
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SENSOR HUB

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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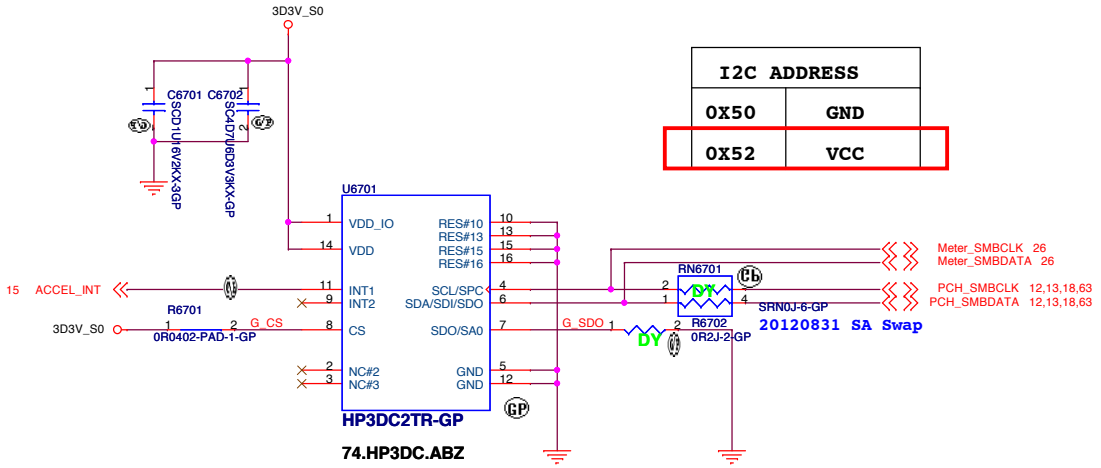
ACCELEROMETER



I2C ADDRESS	
0X50	GND
0X52	VCC

Must be placed in the center of the system

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G Sensor***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (1/5)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Thunderbolt (2/5)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 69 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (3/5)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 70 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (4/5)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (5/5)***

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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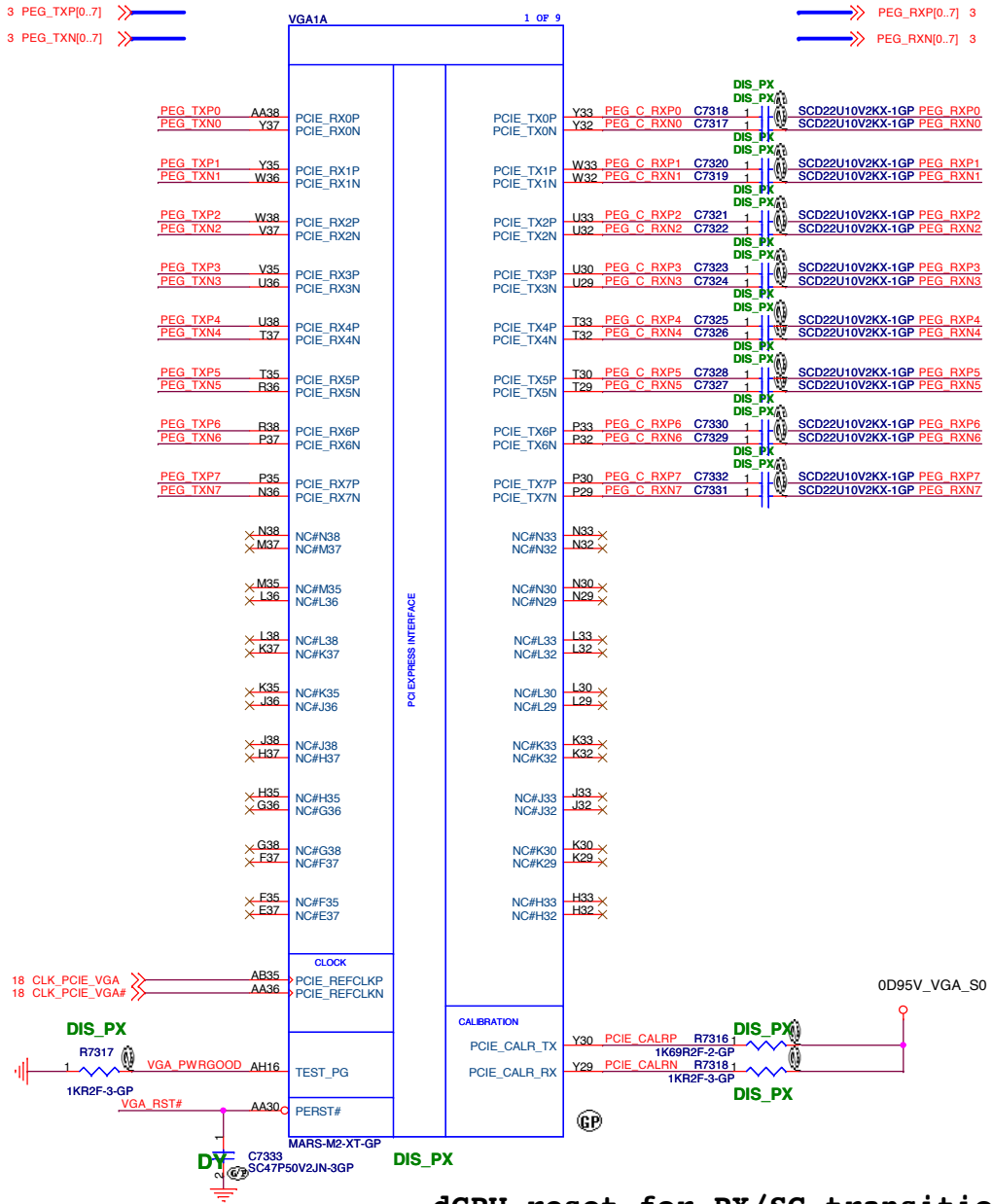

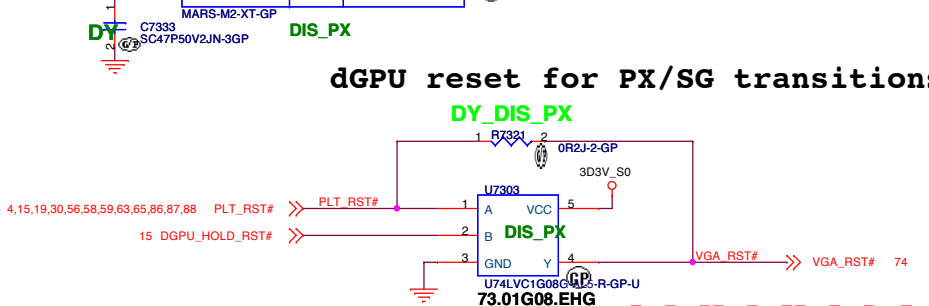

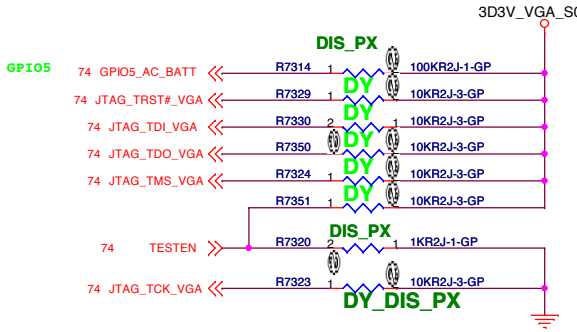

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (1/5) PEG

Size	Document Number	Rev
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Set DVP as 1.8-V (VDDR4/5) general I/O

CTF setpoint is 118°C, and is programmed during ASIC initialization.

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Intel is H_THERMTRIP#

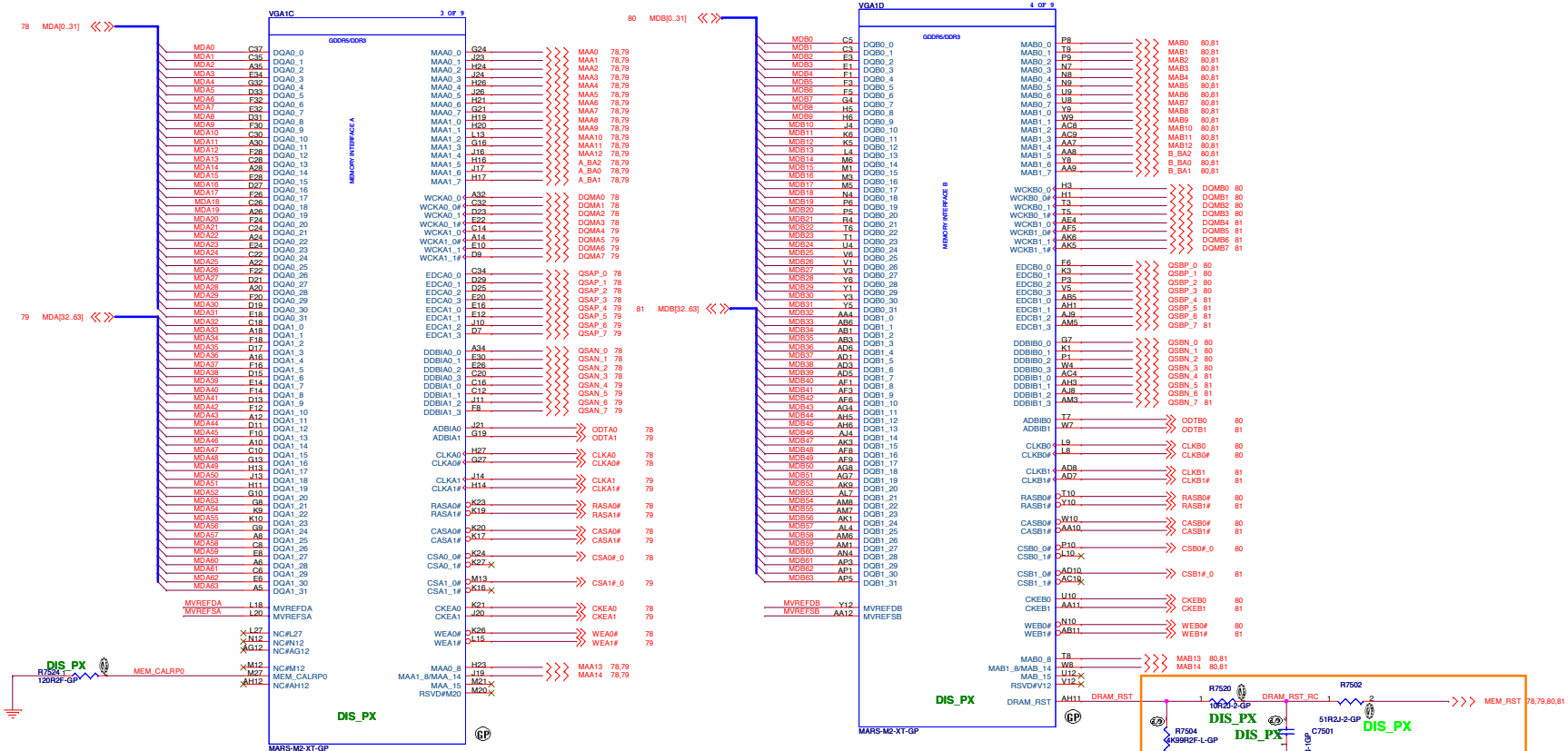
LVDS Interface

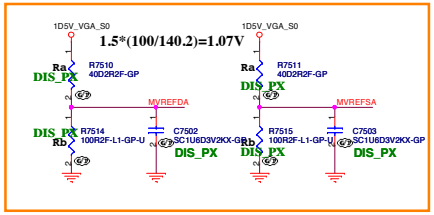
Close to VGA1

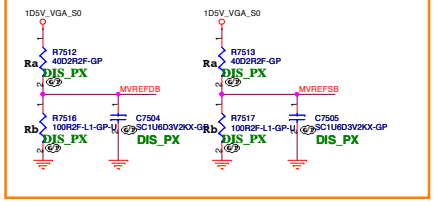
VGA_PS3 VRAM Select
Check table for Select Resistor

VRAM1	VRAM2						
MLPS Bit : PS_3[3:1]			R7427	R7426	Vendor & PN	Die	Process Tech
0	0	0	NC	4750	Samsung K4W1G1646G-BC11	G	35nm
0	0	1	8450	2000	Samsung K4W2G1646E-BC1A	E	20nm
0	1	0	4530	2000	Hynix H5TQ1G63EFR-11C	E	36nm
0	1	1	6980	4990	Hynix H5TC2G63FFR-11C	F	29nm/JAN13
SI Stage							
1	0	1	3240	5620	Micron MT41J128M16JT-093G:K	K	30nm
SI Stage							
NC	NC	NC	3400	10000	UMA		
Vendor ID 00=Samsung 01=Hynix 10=Micron			0=64M 1=128M				

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU (2/5) DIGITALOUT
Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1
Date: Monday, August 12, 2013 | Sheet 74 of 103







This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

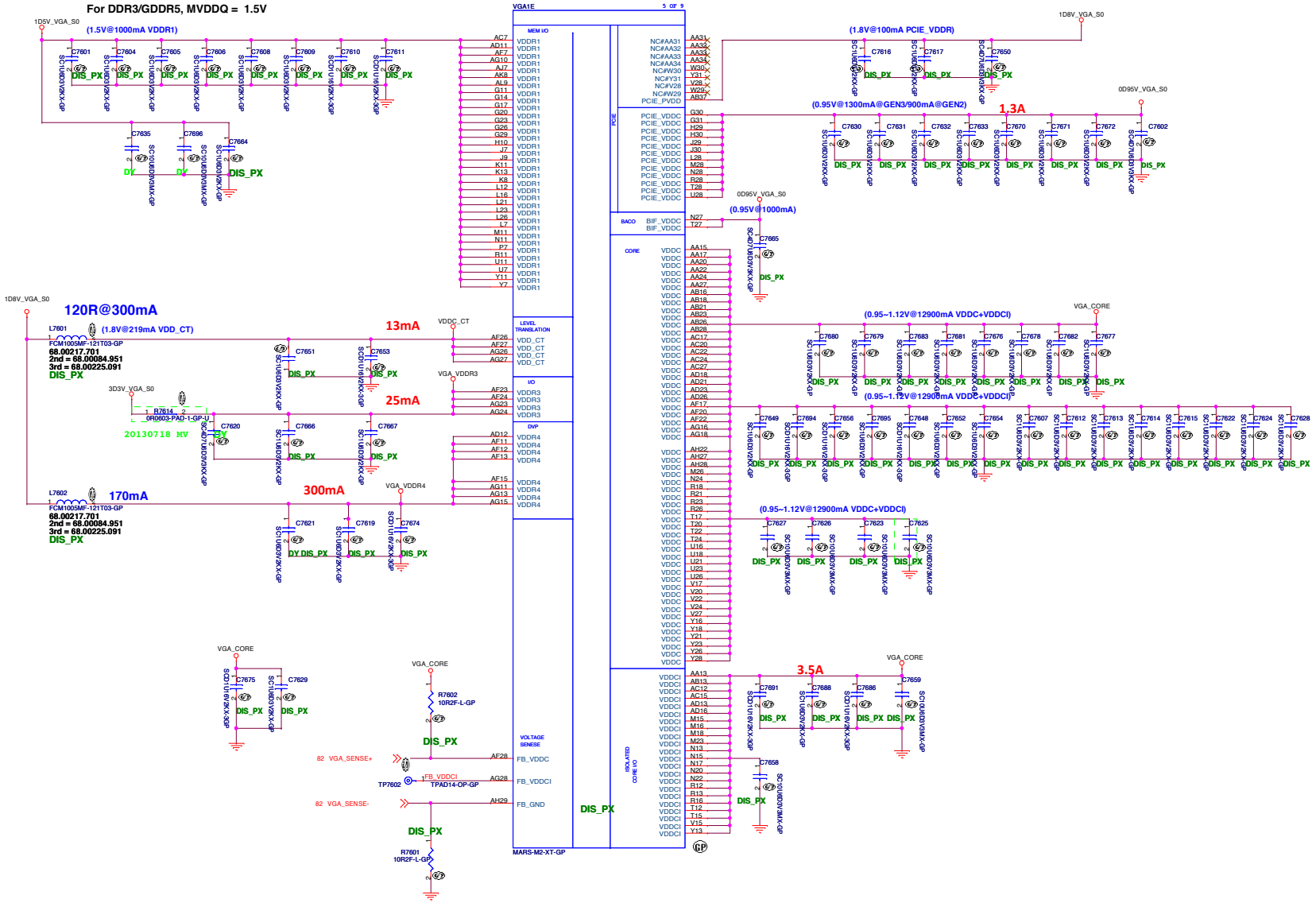
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (3/5) VRAM I/F

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 75 of 103



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (4/5) PWR

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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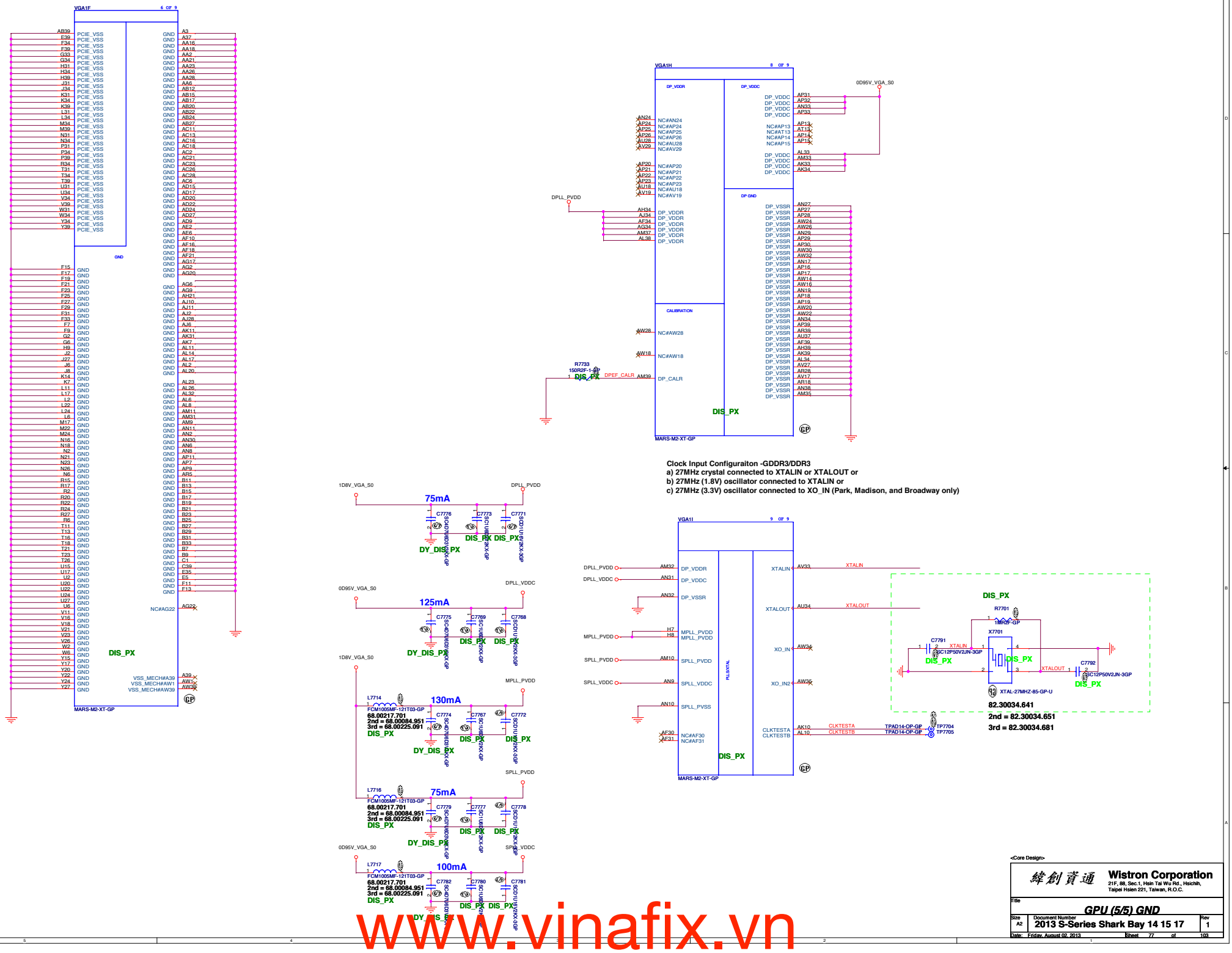
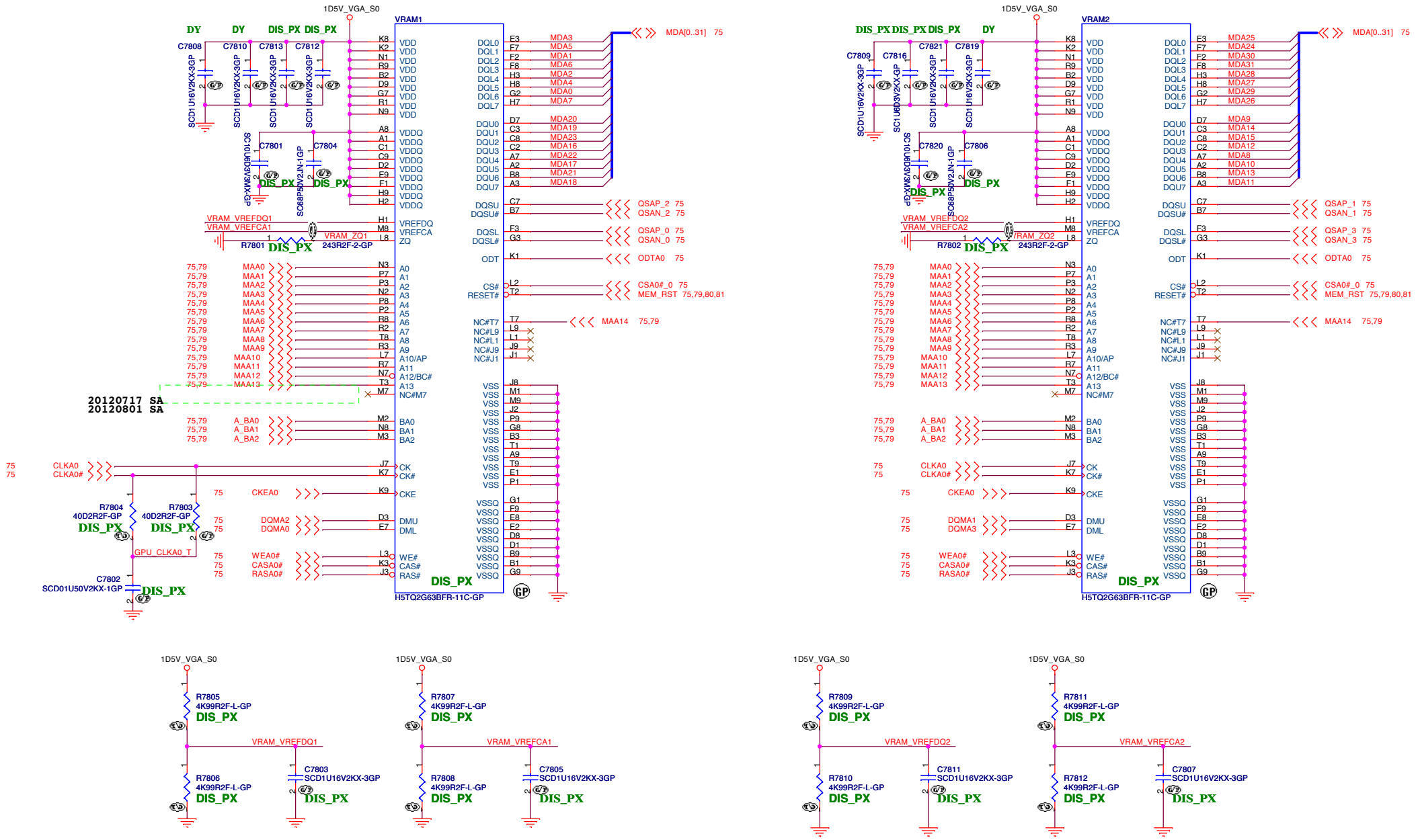


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (5/5) GND

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

Date: Friday, August 02, 2013 Sheet 77 of 103



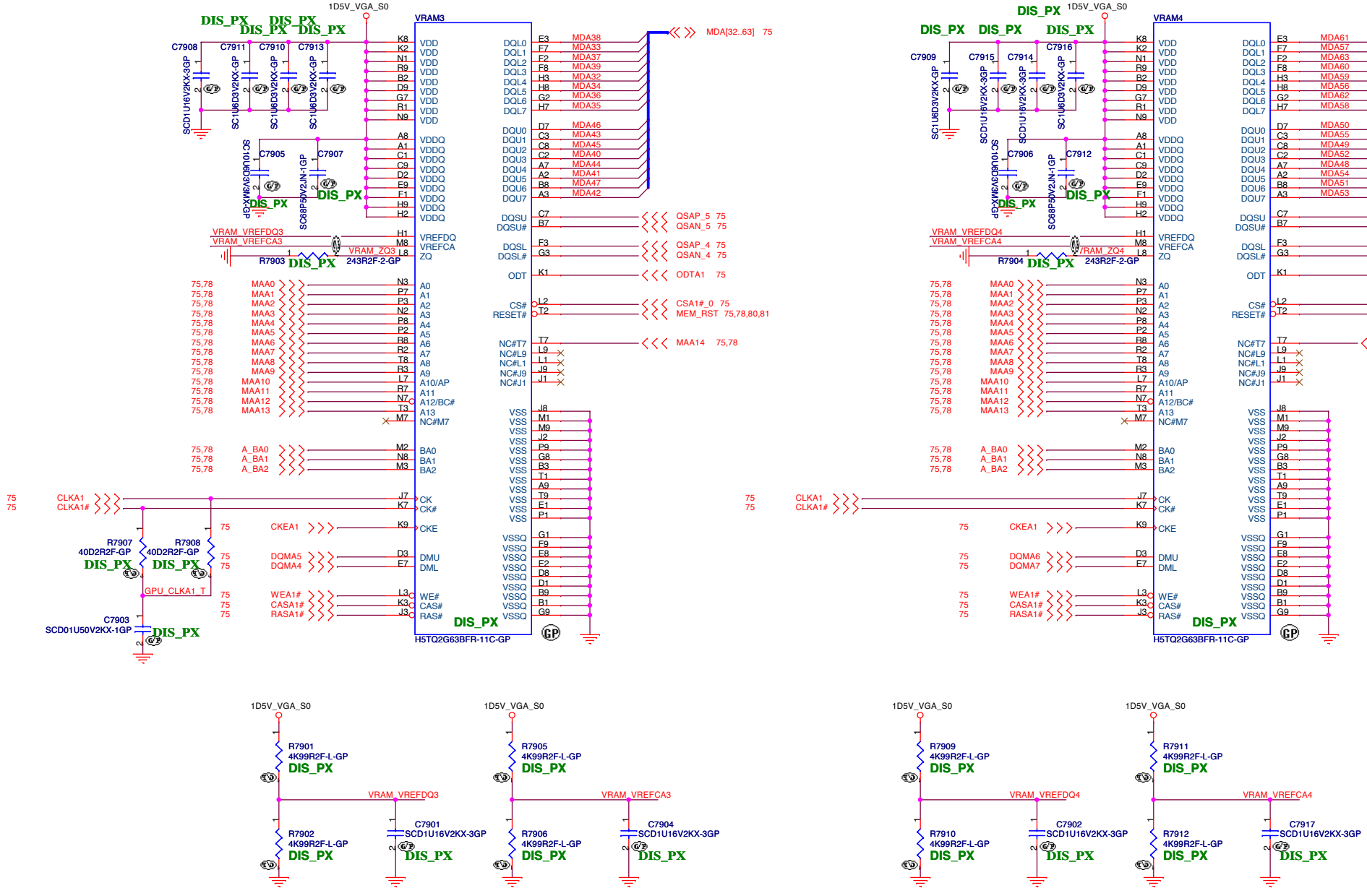
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM1,2 (1/4)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 78 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM3,4 (2/4)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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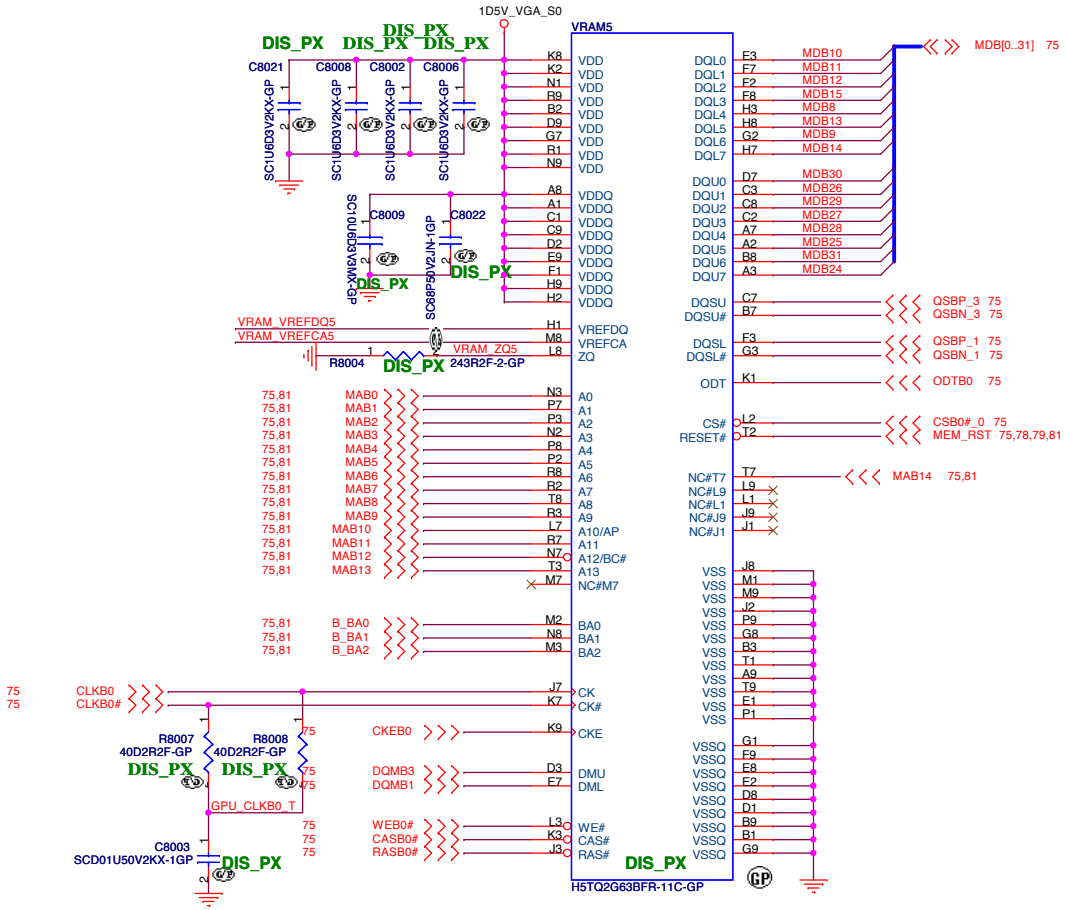

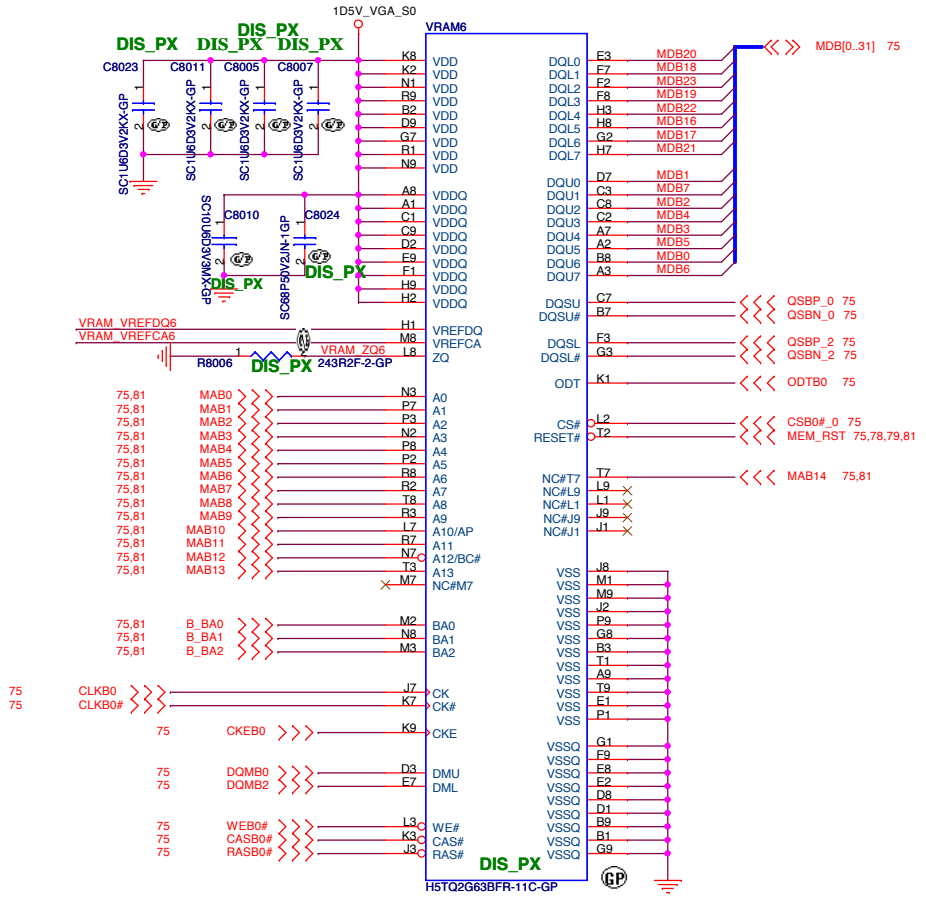

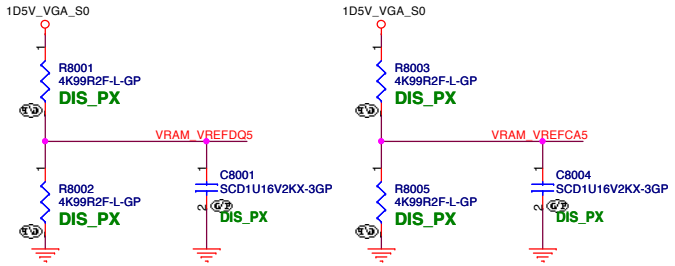

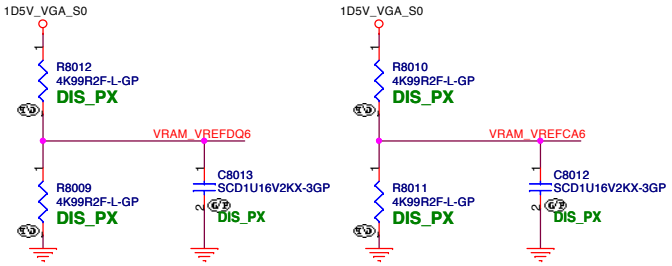

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM5,6 (3/4)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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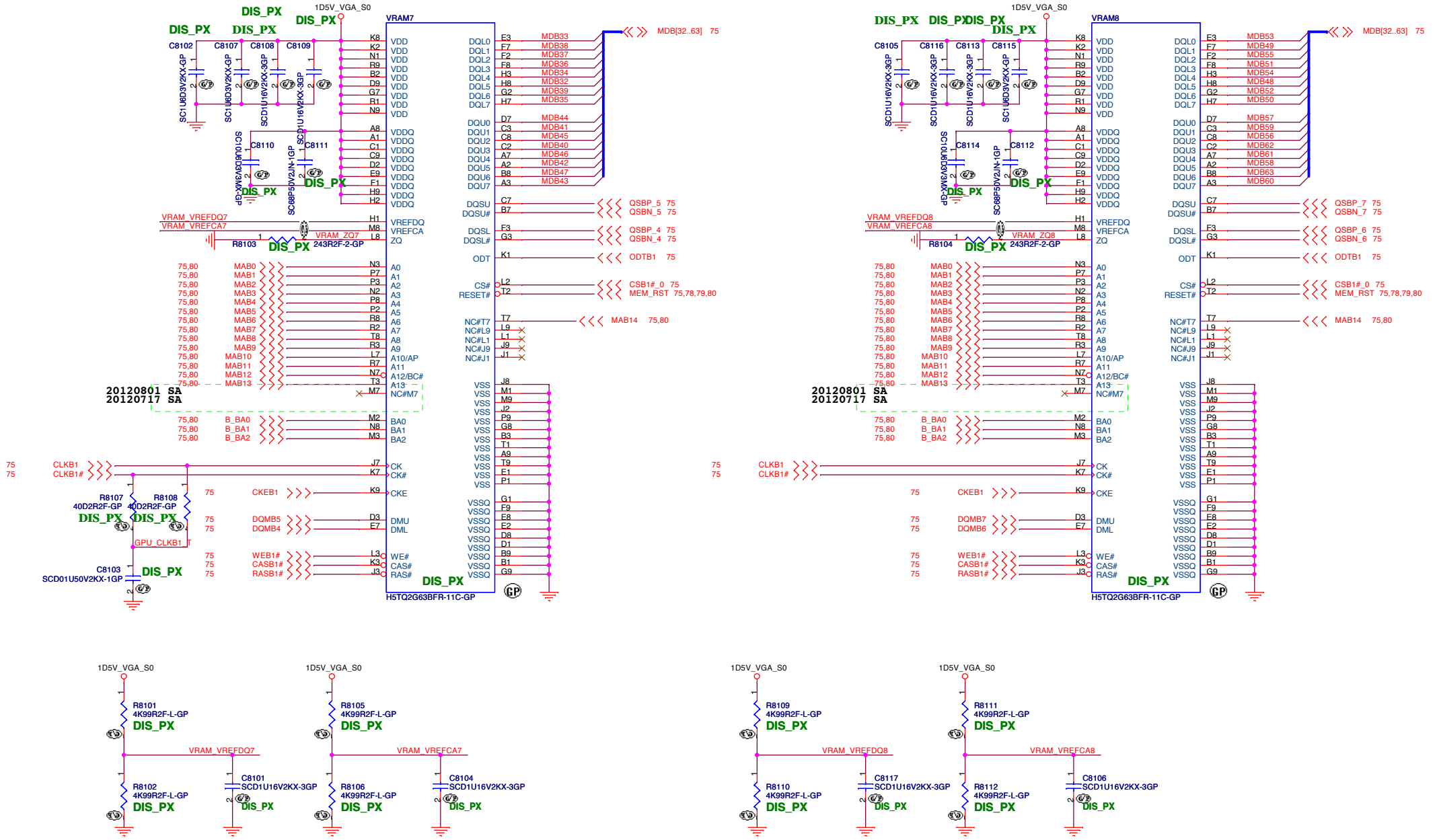

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM7,8 (4/4)
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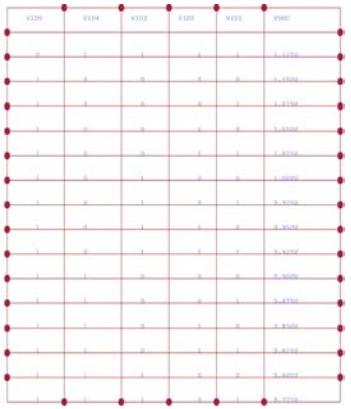
SSID = PWR.Plane.Regulator_vga_core

V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.85V	0	0	1	0	1	1	0



Design Current = 27A
OCP>55A

20121011 Delete R8201 C8201

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE

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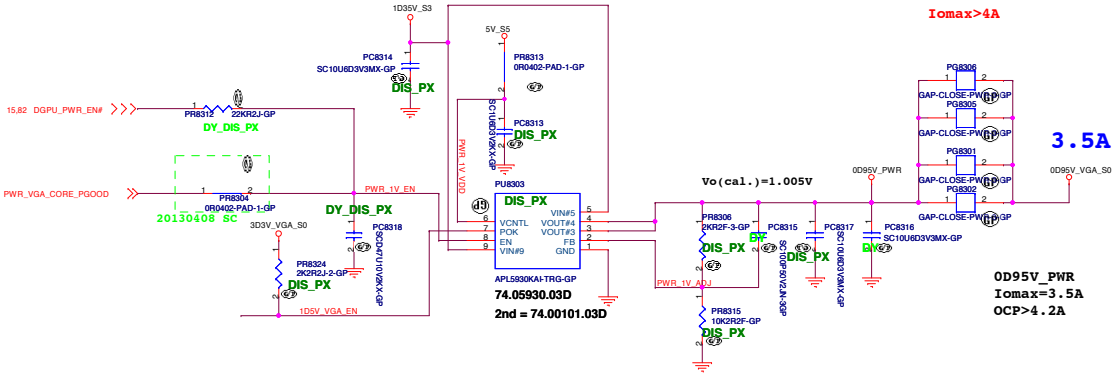
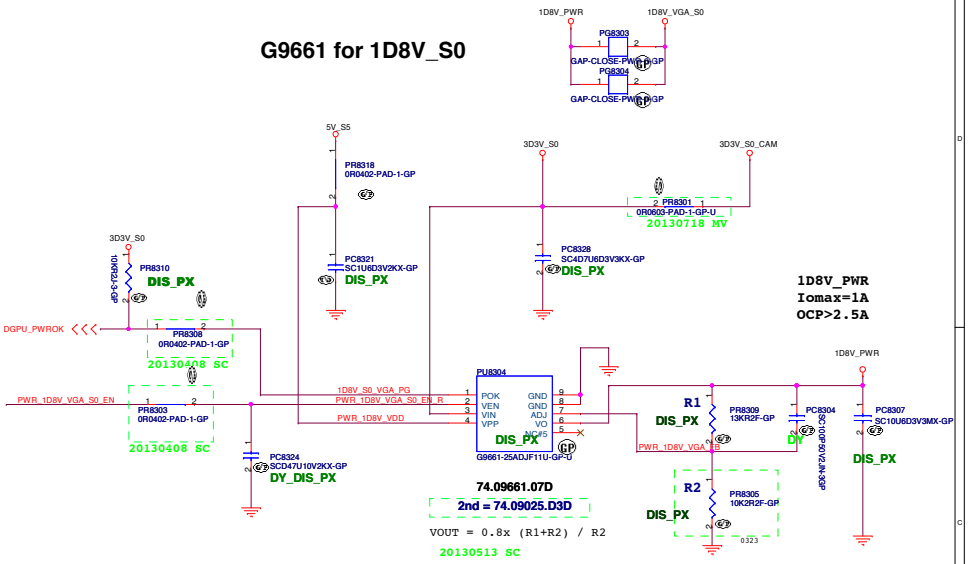
3D3V_VGA_S0 > VGA_CORE > 0D95V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0

0D95V_S0

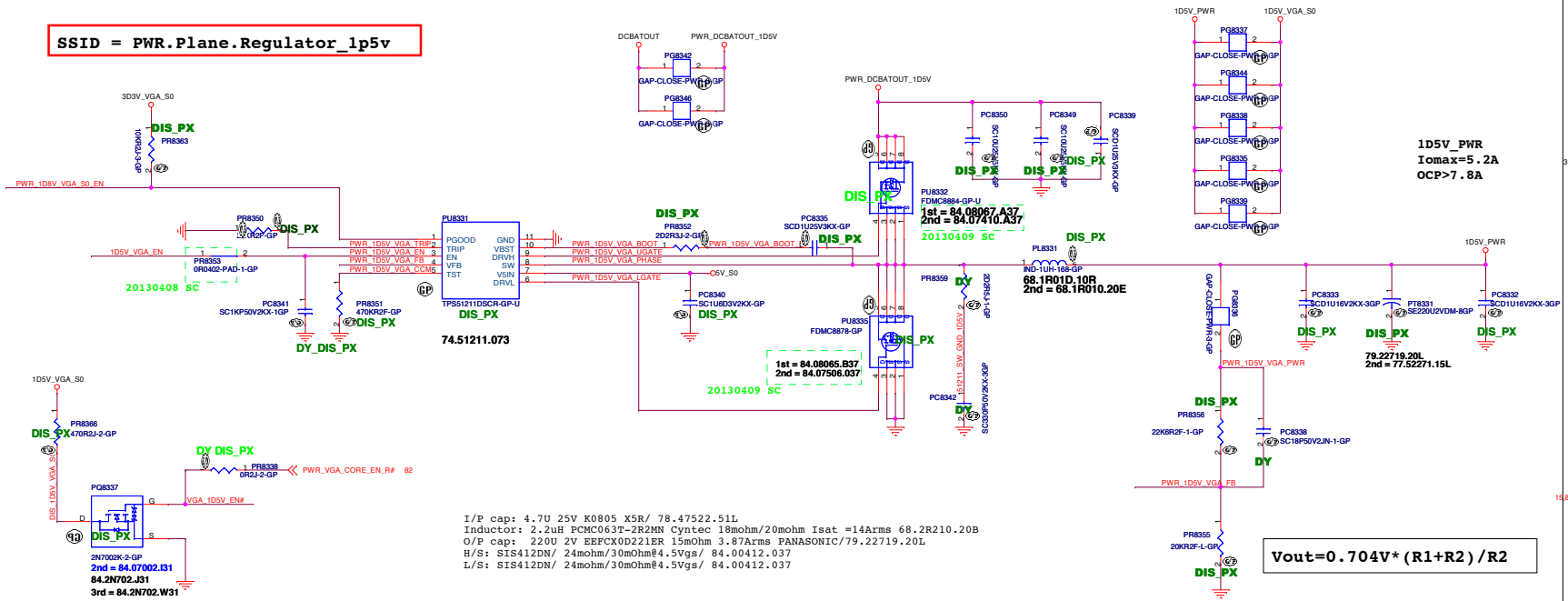


G9661 for 1D8V_S0



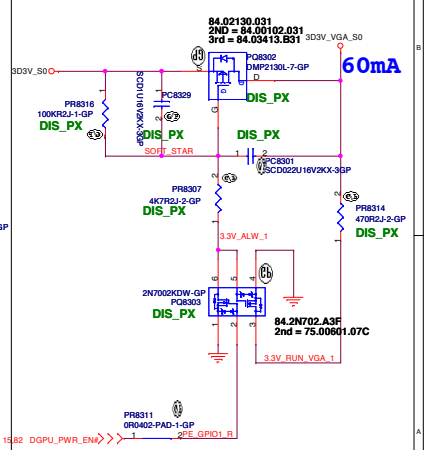
SSID = PWR.Plane.Regulator_1p5v

1D5V_PWR



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

3D3V_VGA_S0



<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: DISCRETE VGA POWER
Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1
Date: Monday, August 12, 2013 | Sheet 83 of 103

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU Memory(2/5)***
Size: A2	Document Number: **2013 S-Series Shark Bay 14 15 17** Rev: 1A
Date: Wednesday, July 03, 2013	Sheet 84 of 103

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU DP/LVDS/CRT/GPIO(3/5)

Size: A4 | Document Number: 2013 S-Series Shark Bay 14/15/17 | Rev:

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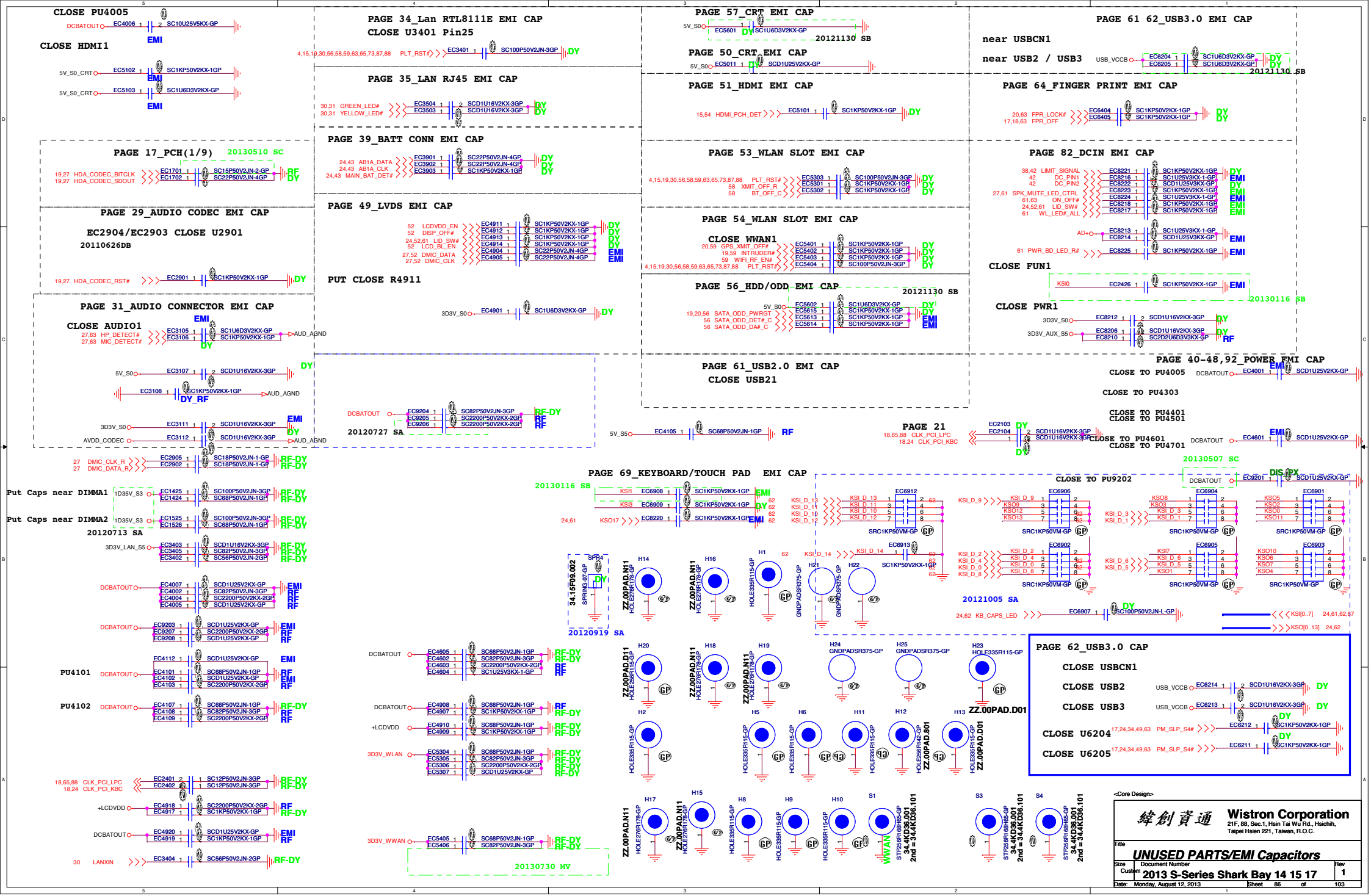
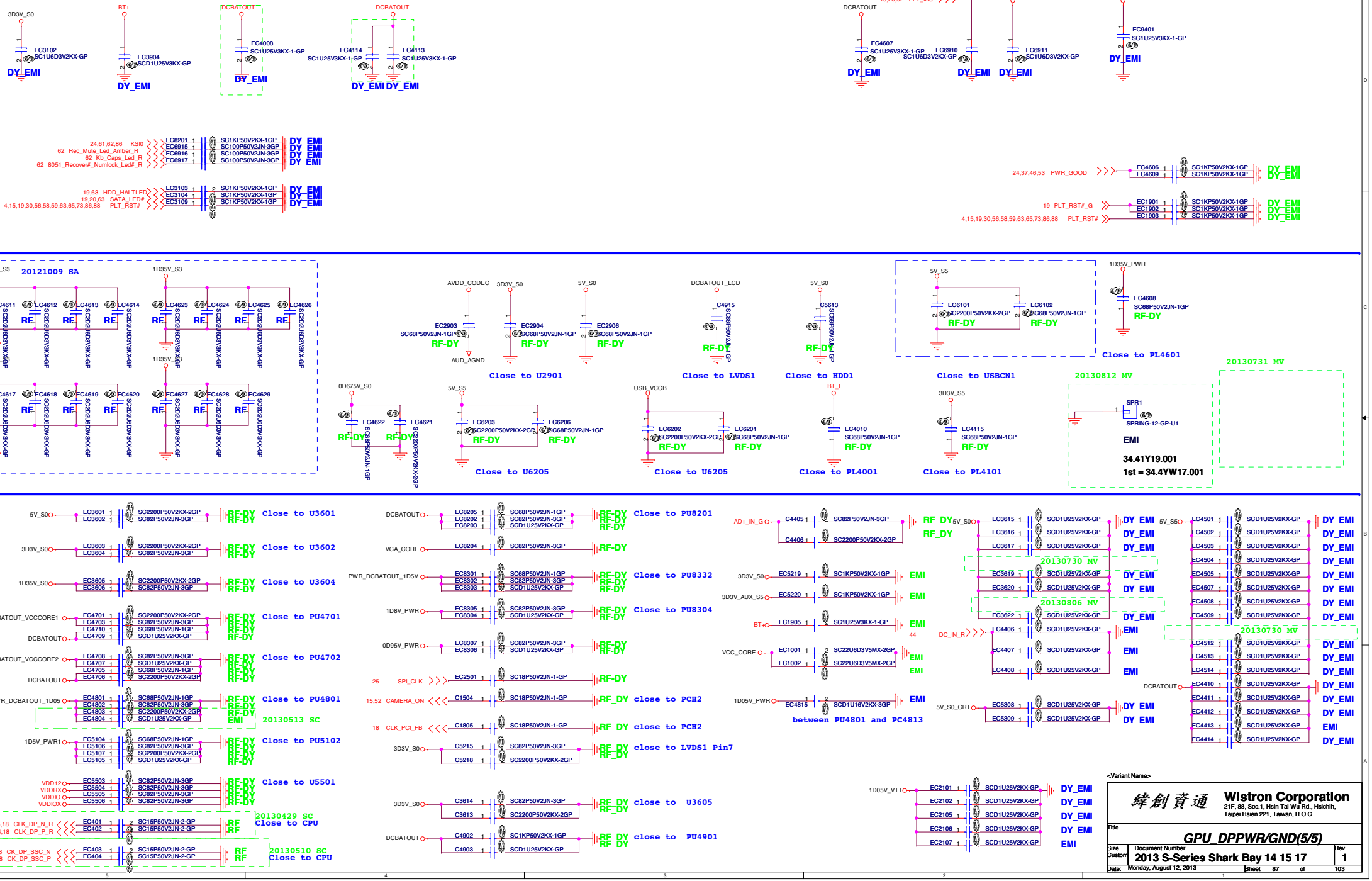


EMI Caps



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>
Title: GPU_DPPWR/GND(5/5)
Size: Custom
Document Number: 2013 S-Series Shark Bay 14 15 17
Rev: 1
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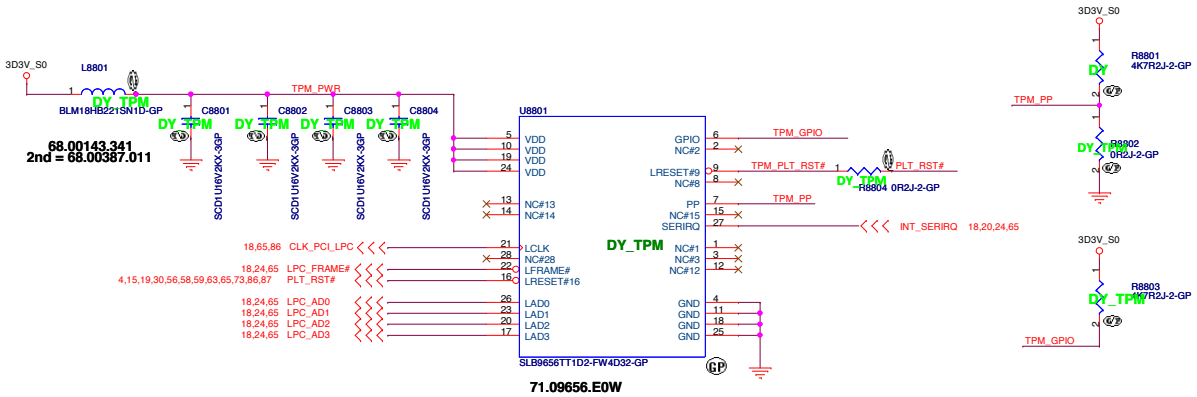

20130730 MV

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***TPM***
Size: Custom	Document Number: 2013 S-Series Shark Bay 14/15 17
Date: Monday, August 12, 2013	Sheet 88 of 103

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Finger Print Conn

Size	Document Number	Rev
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev:

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7.8 (4/4)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14/15/17 | Rev:

Date: Wednesday, July 03, 2013 | Sheet 91 of 103

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP3218 VGACORE25W

Size: A2 | Document Number: 2013 S-Series Shark Bay 14'15 17 | Rev:

Date: Wednesday, July 03, 2013 | Sheet 92 of 103

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev:

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev:

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Shark Bay SV

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_XDP***

Size	Document Number	Rev
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

Size: A3 | Document Number: **2013 S-Series Shark Bay 14'15 17** | Rev:

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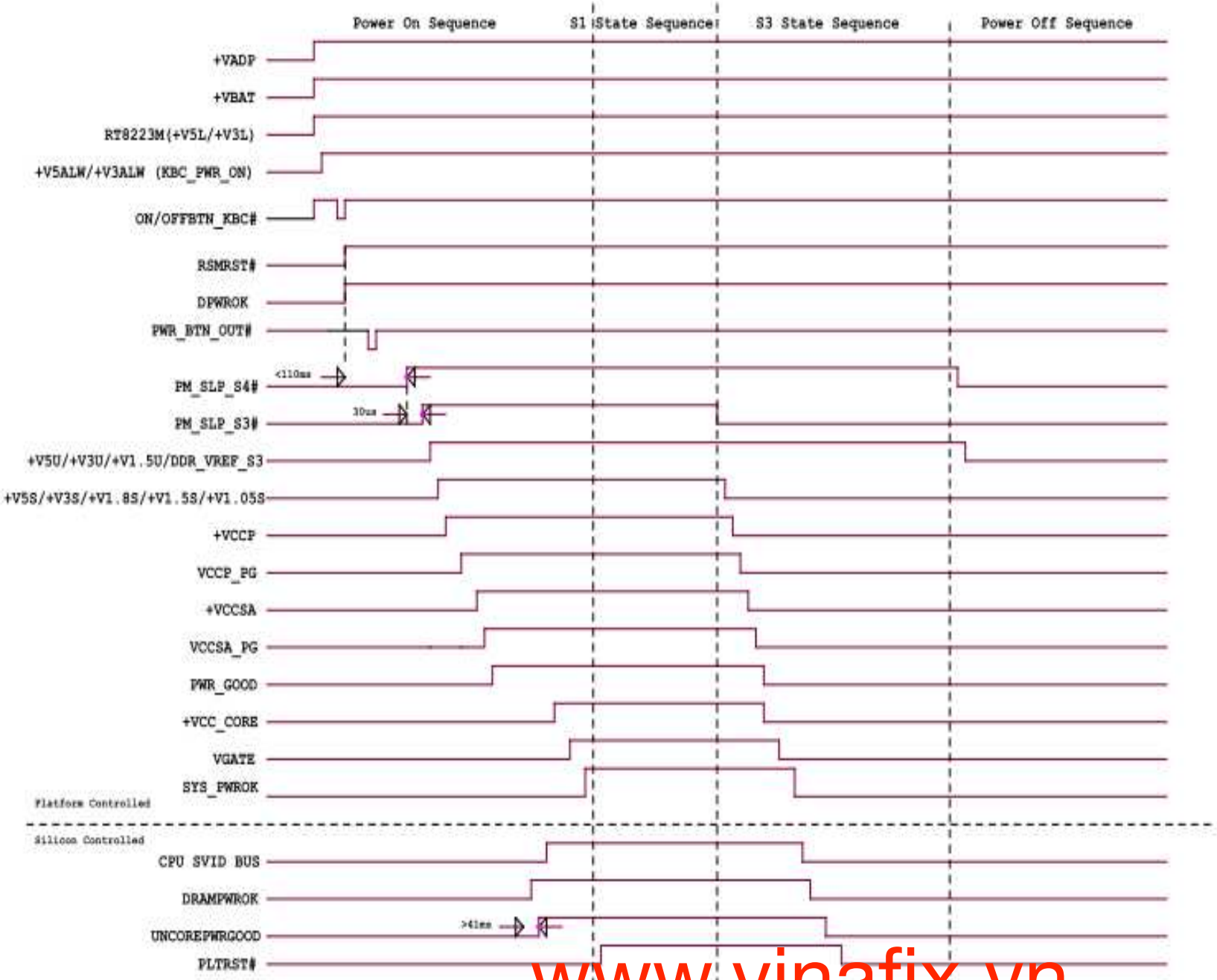
S-Series Power Sequence and Reset Signal Timing



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Sequence***

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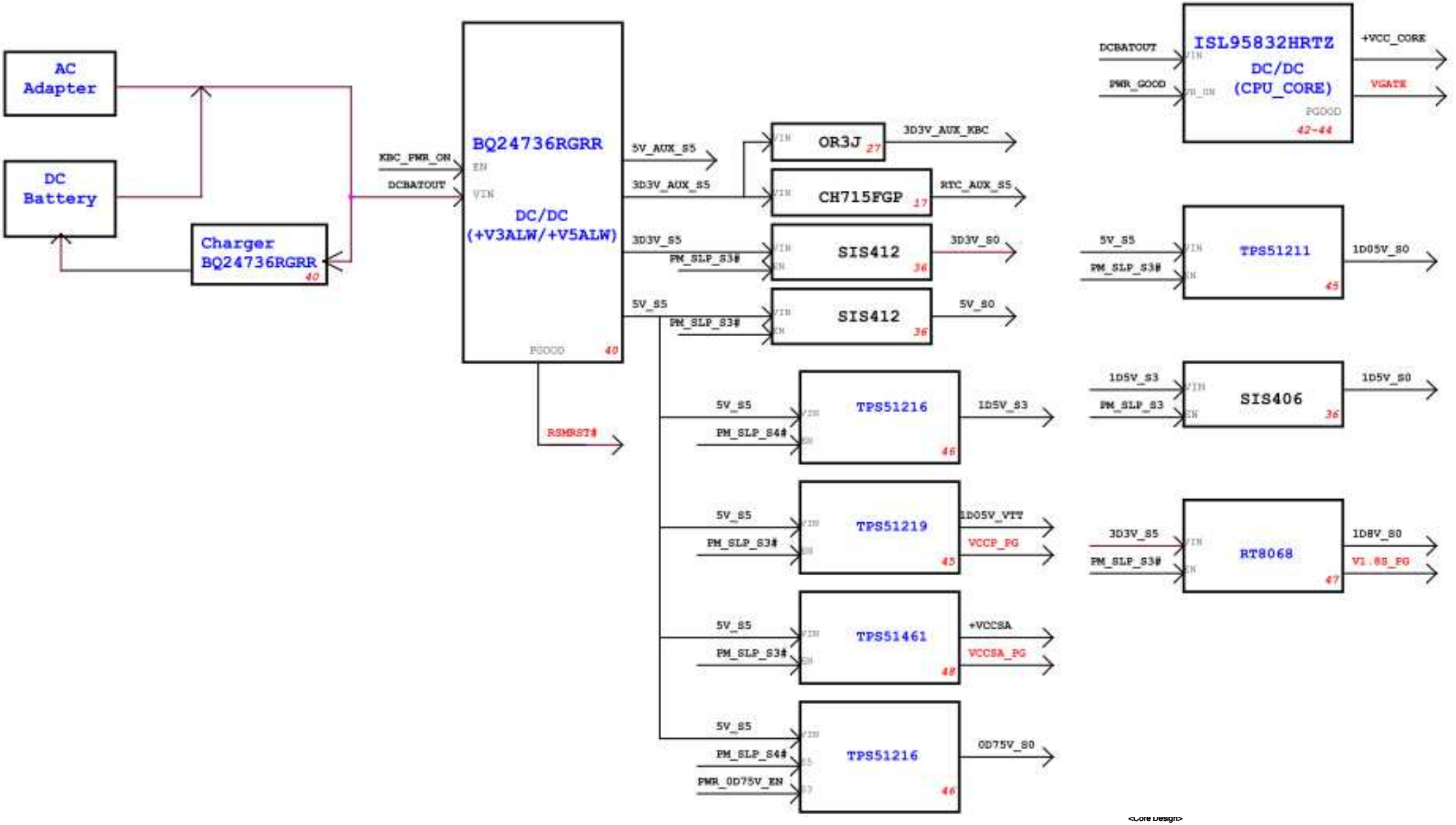
S-Series POWER BLOCK DIAGRAM



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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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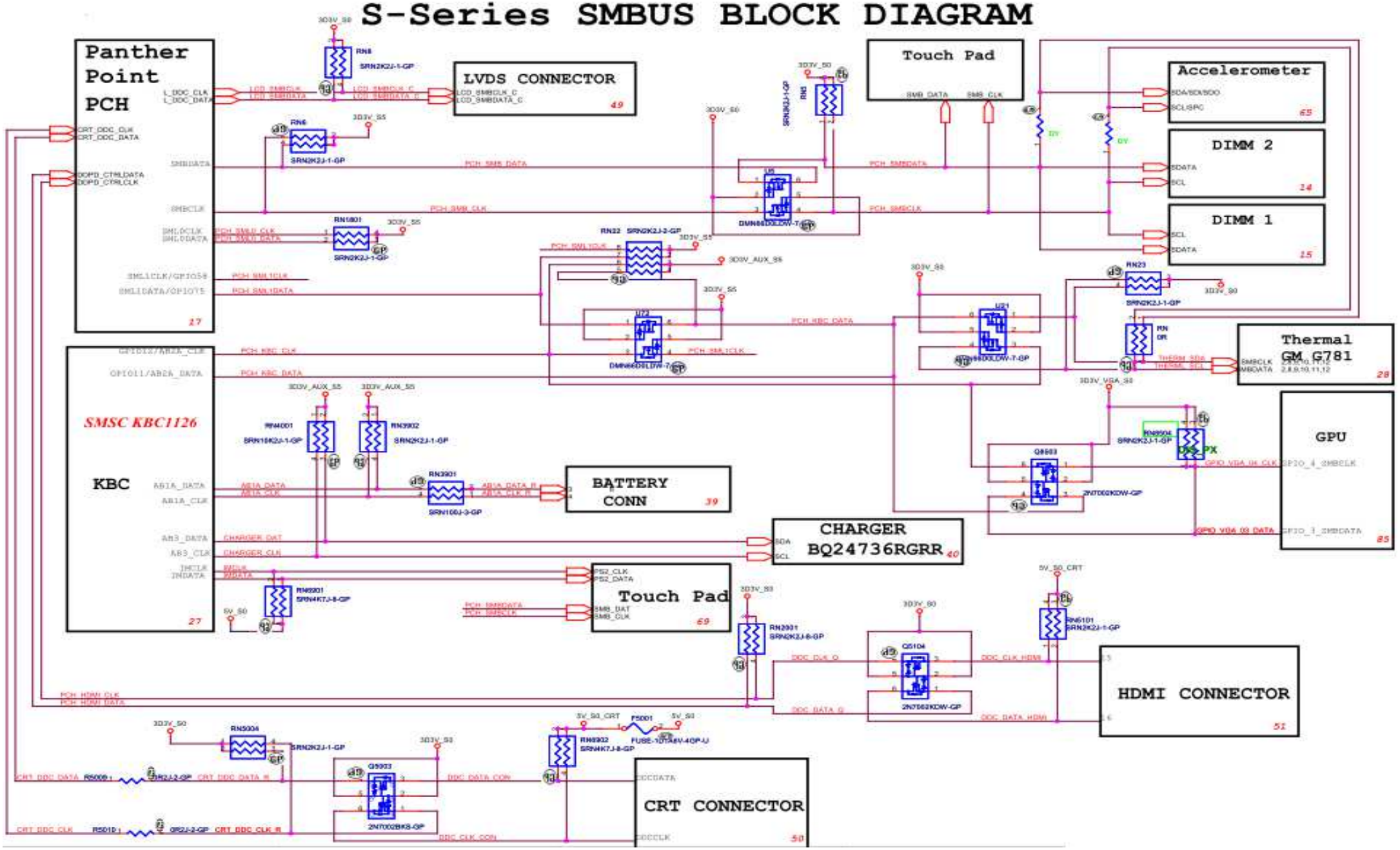
S-Series SMBUS BLOCK DIAGRAM



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SMBUS Block Diagram***

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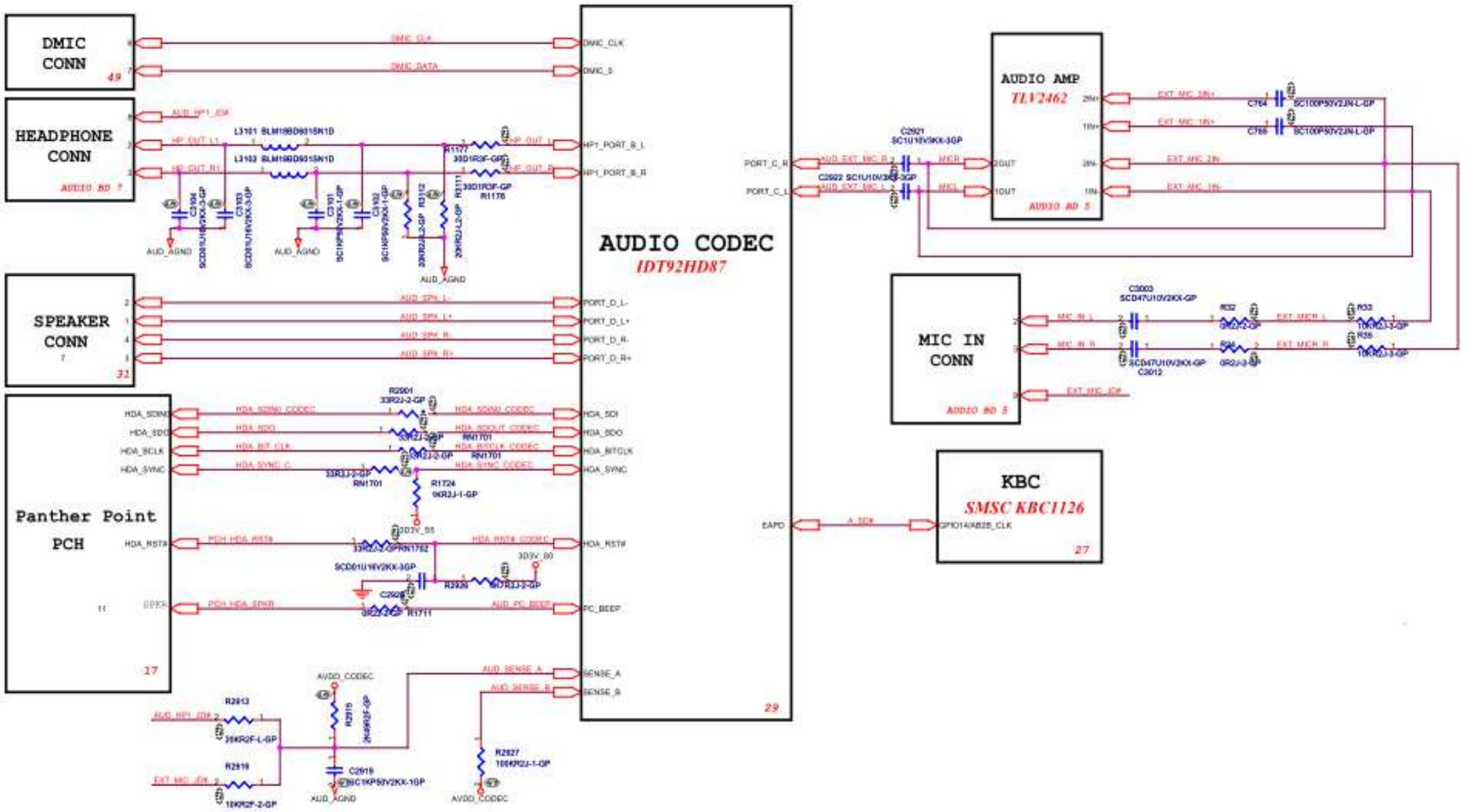
S-Series AUDIO BLOCK DIAGRAM



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA

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